

FIG. 2

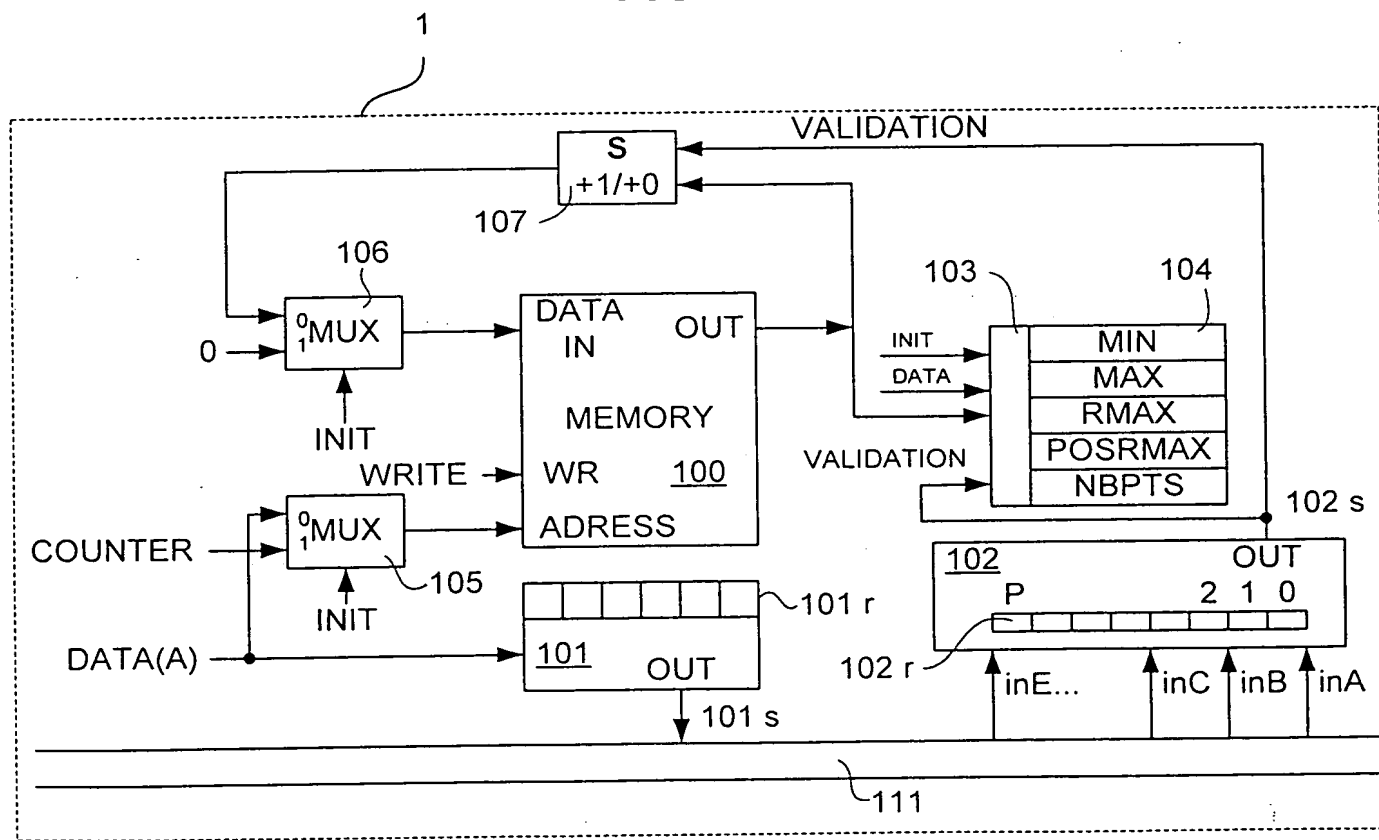


FIG. 3

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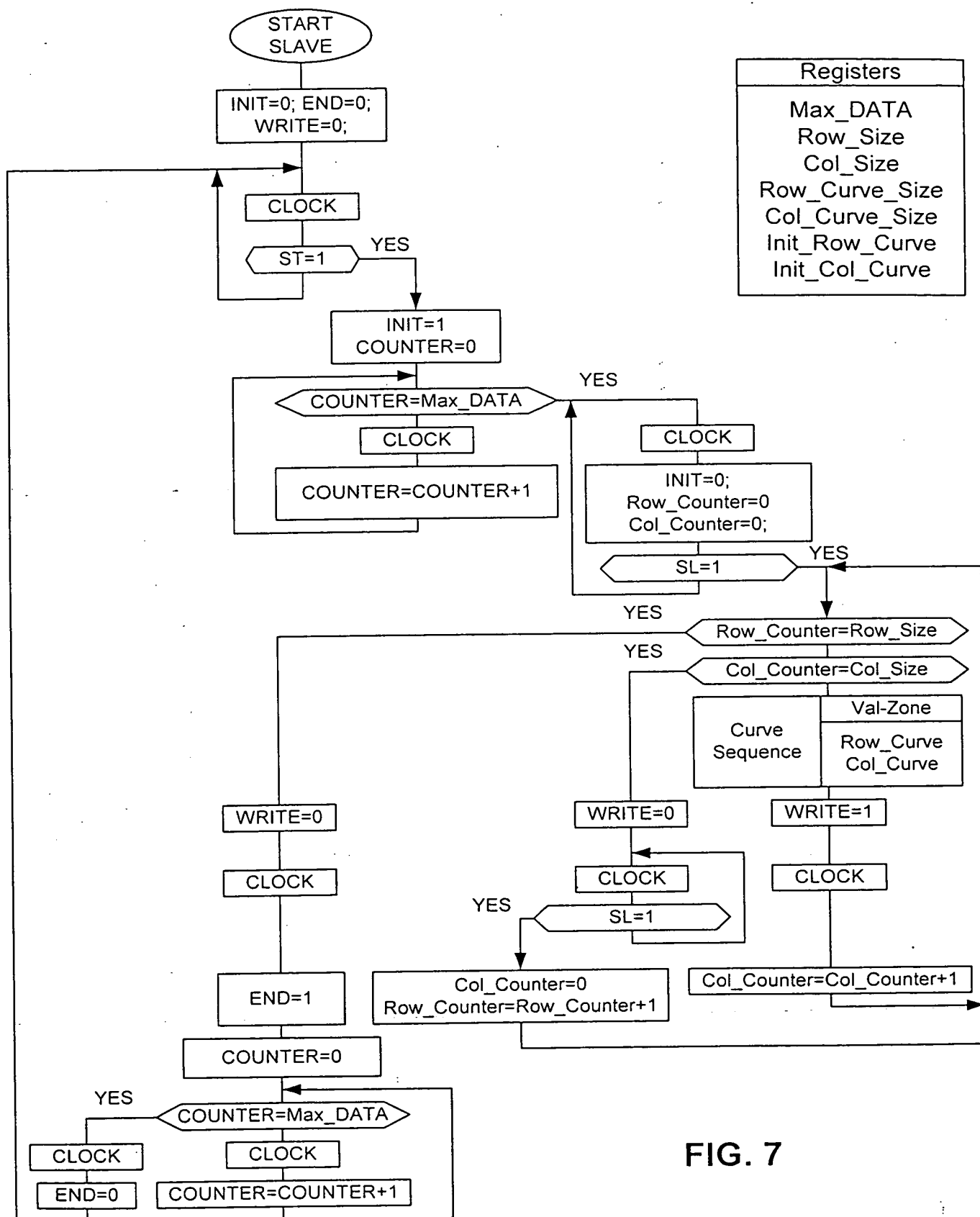
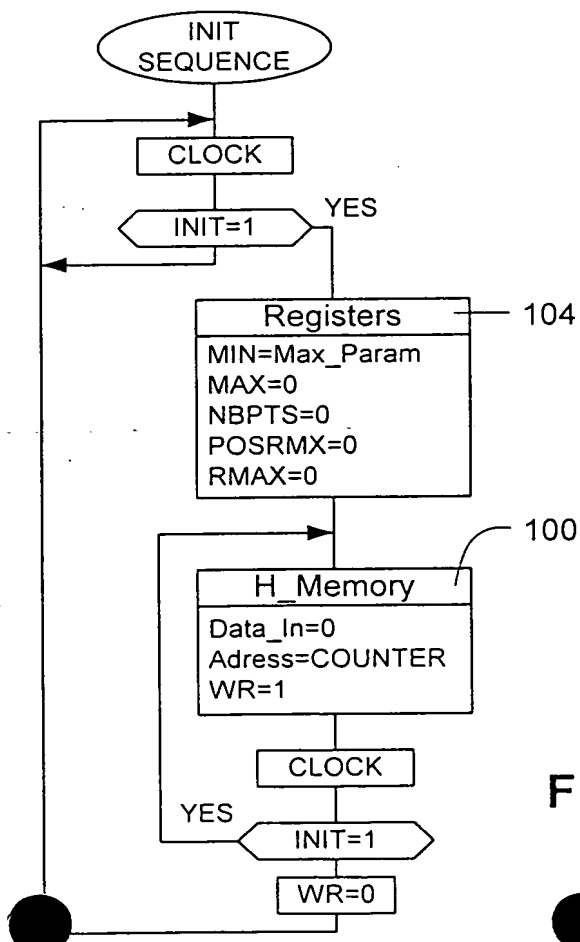
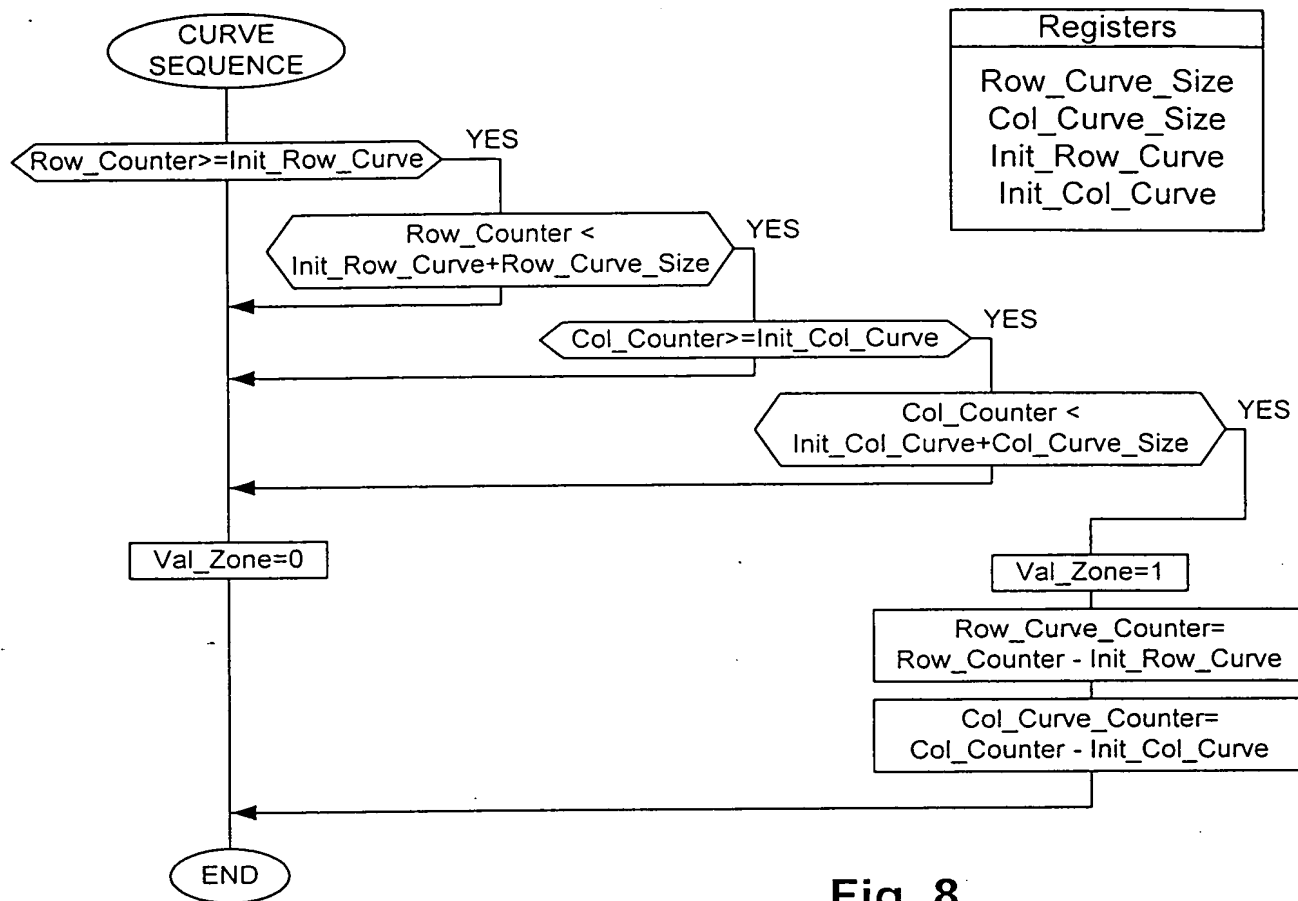


FIG. 7

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096786-0301

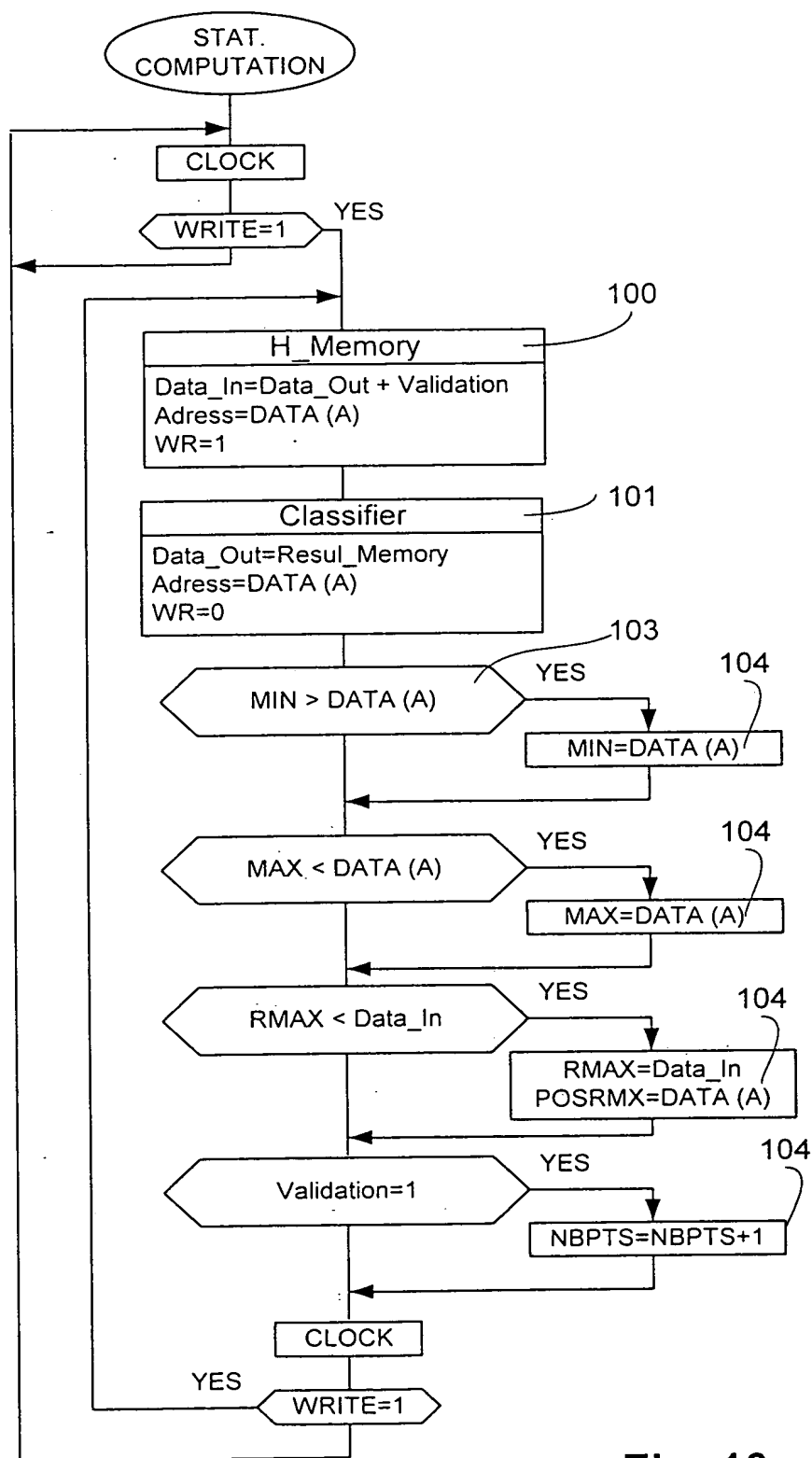


Fig. 10

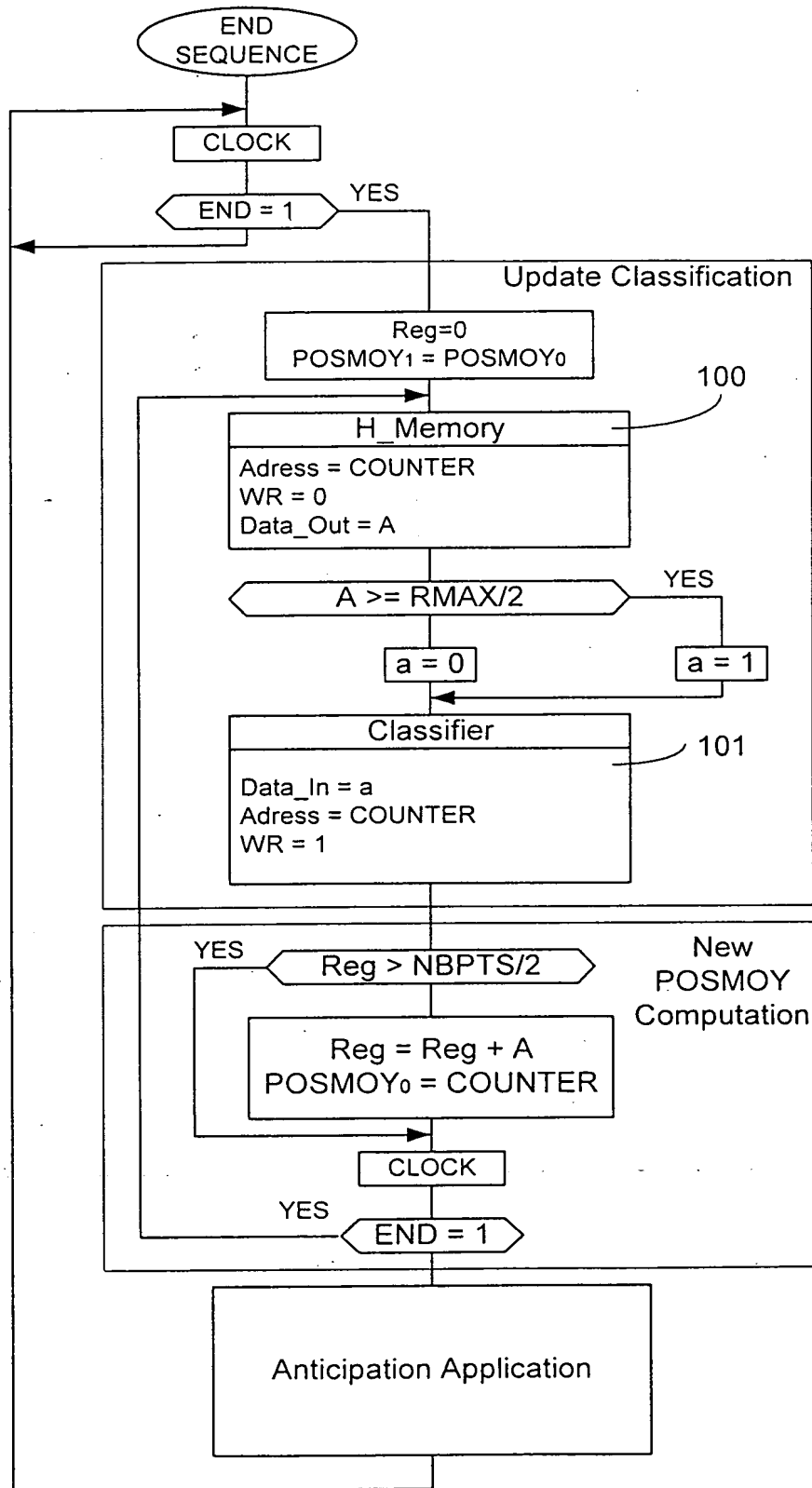


Fig. 11

FIG. 12 is a block diagram of a memory system. It features two memory units, 100 and 118, each with a DATA IN, DATA OUT, MEMORY, WR (Write Enable), and ADDRESS input. The system includes two multiplexers (MUX) and two AND gates. The top MUX (105) selects between two DATA (A) COUNTER inputs and its output is connected to the ADDRESS input of memory unit 100. Its WR input is connected to an AND gate (113), which also receives an INIT signal. The bottom MUX (108) similarly selects between two DATA (A) COUNTER inputs and connects to the ADDRESS input of memory unit 118. Its WR input is connected to an AND gate (112), which also receives an INIT signal. Both AND gates (112 and 113) have an END signal input. The output of memory unit 100 is connected to a block 101, which contains a 1/2 divider and a P > Q comparator. Block 101 is also connected to a block 104, which outputs RMAX and NBPTS signals. The output of memory unit 118 is connected to a block 115, which contains a P > Q comparator and a 1/2 divider. Block 115 is connected to a block 119, which outputs an END signal to the WR input of memory unit 118. The output of memory unit 118 is also connected to a block 119s, which outputs an END signal to the WR input of memory unit 100. The output of memory unit 100 is also connected to a block 119, which outputs an END signal to the WR input of memory unit 118.

FIG. 12

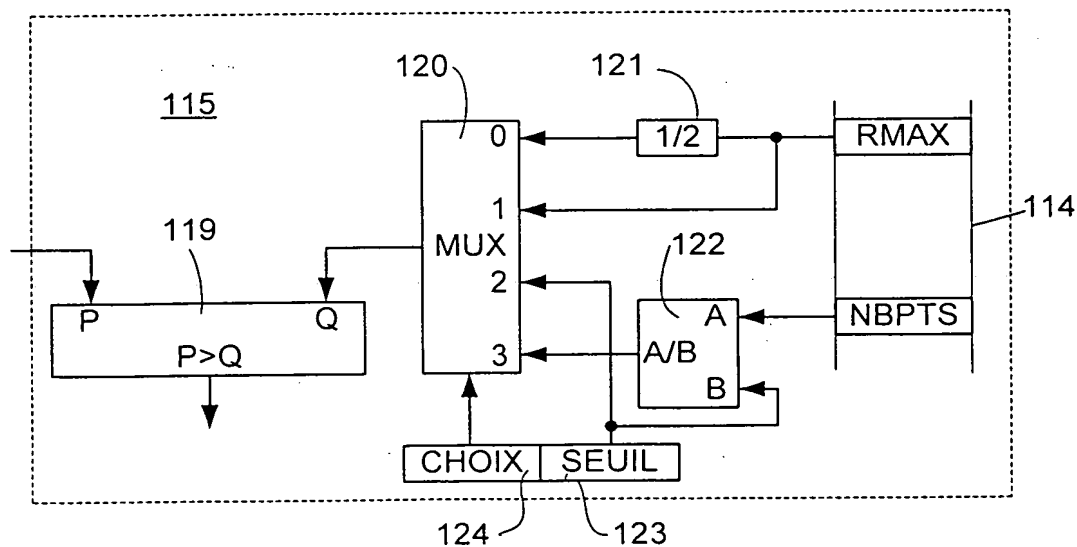
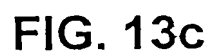


FIG. 13



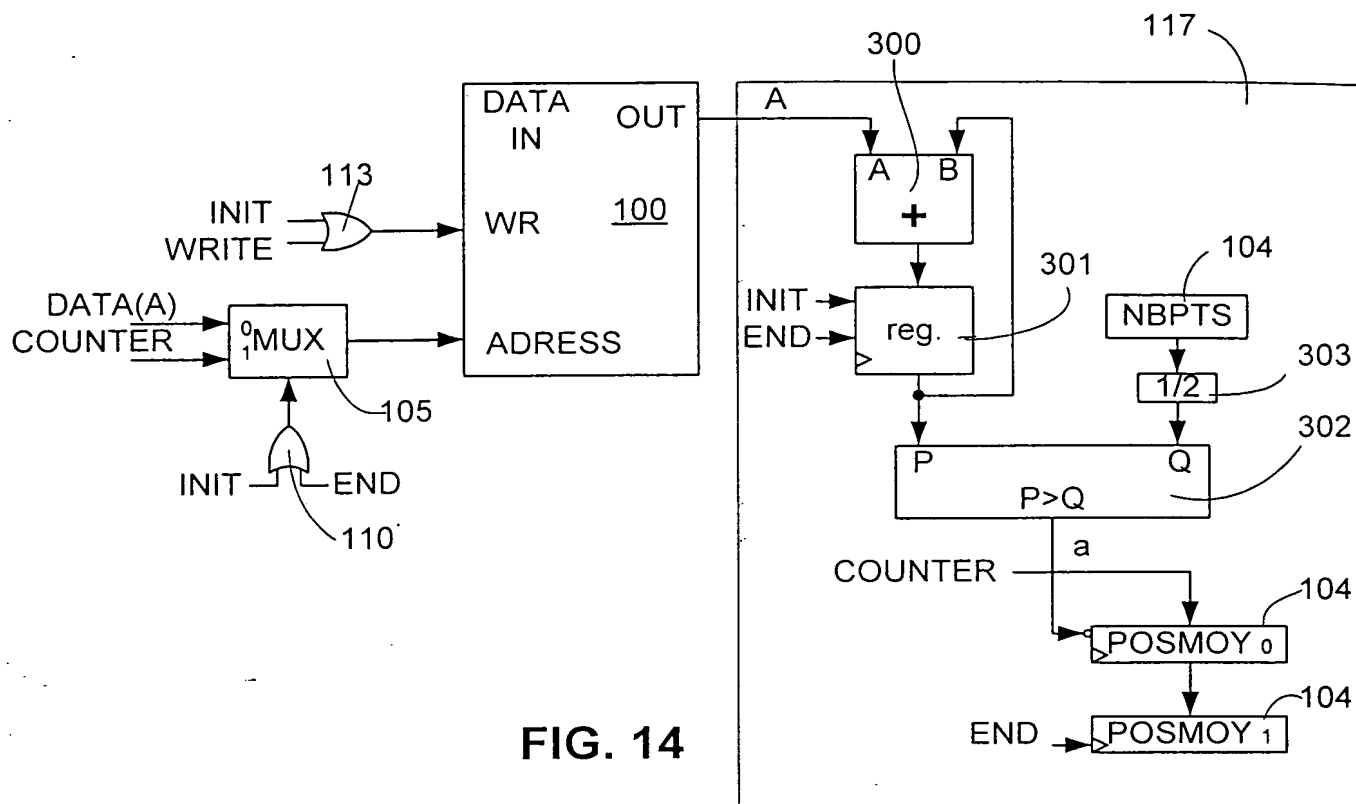


FIG. 14

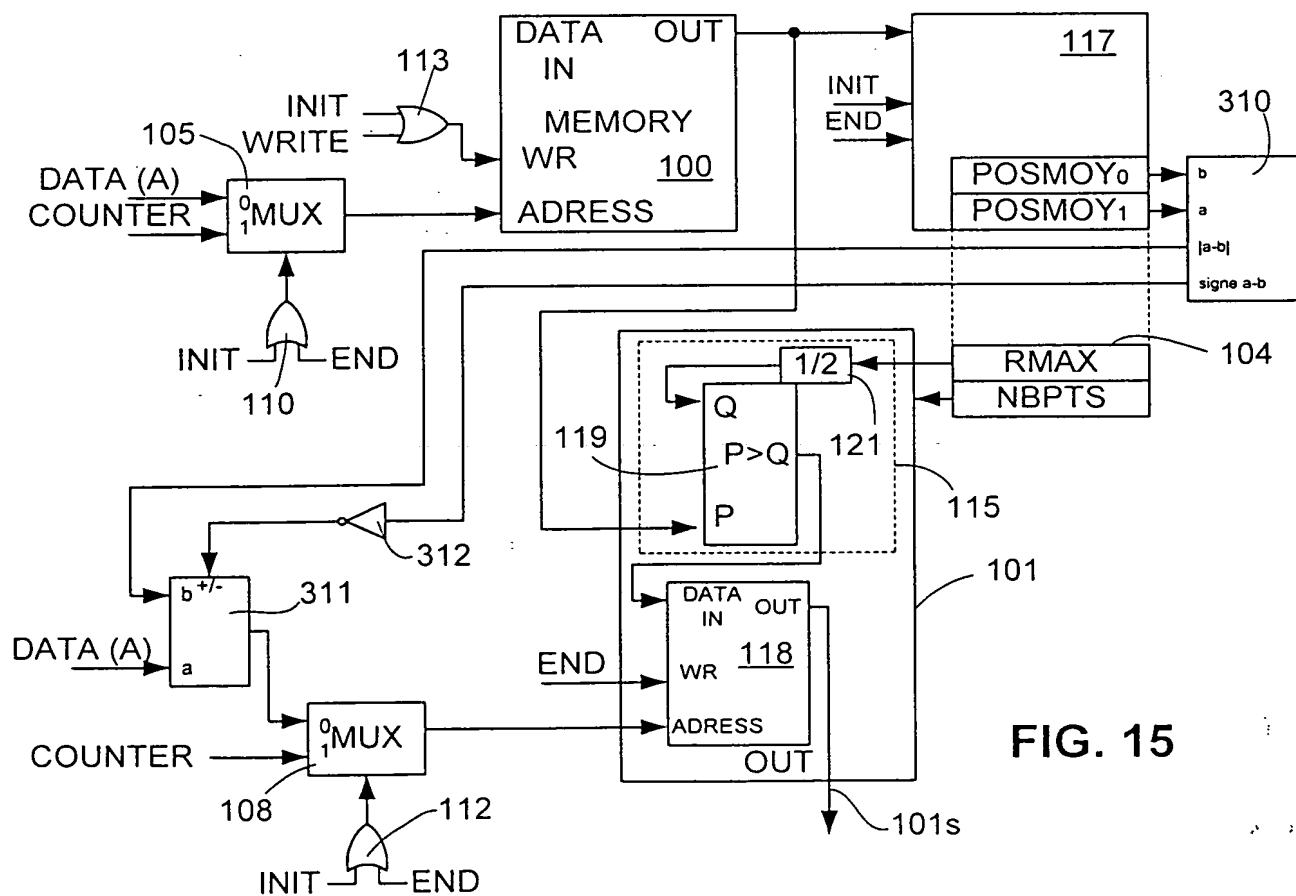


FIG. 15

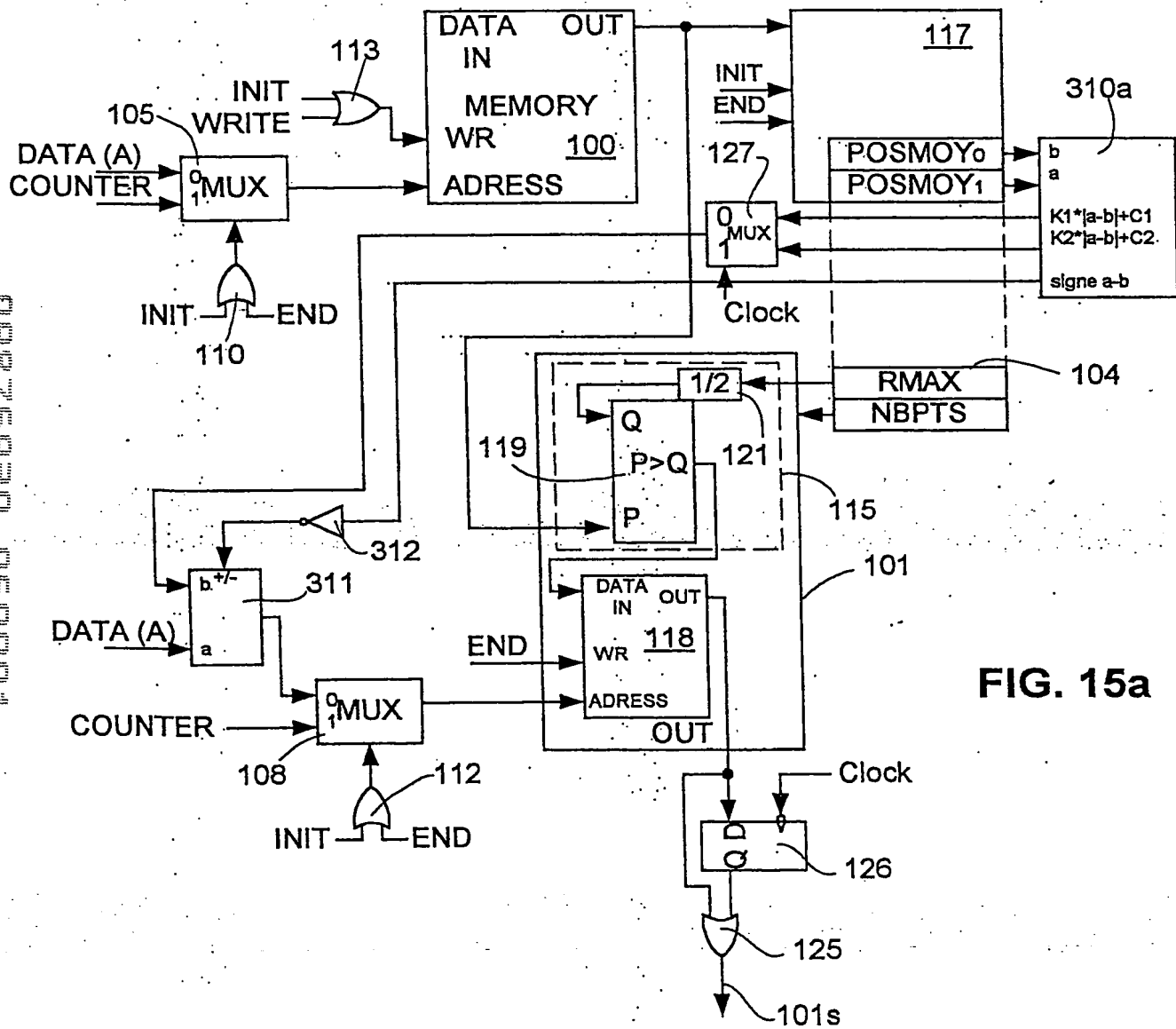


FIG. 15a

FIG. 16

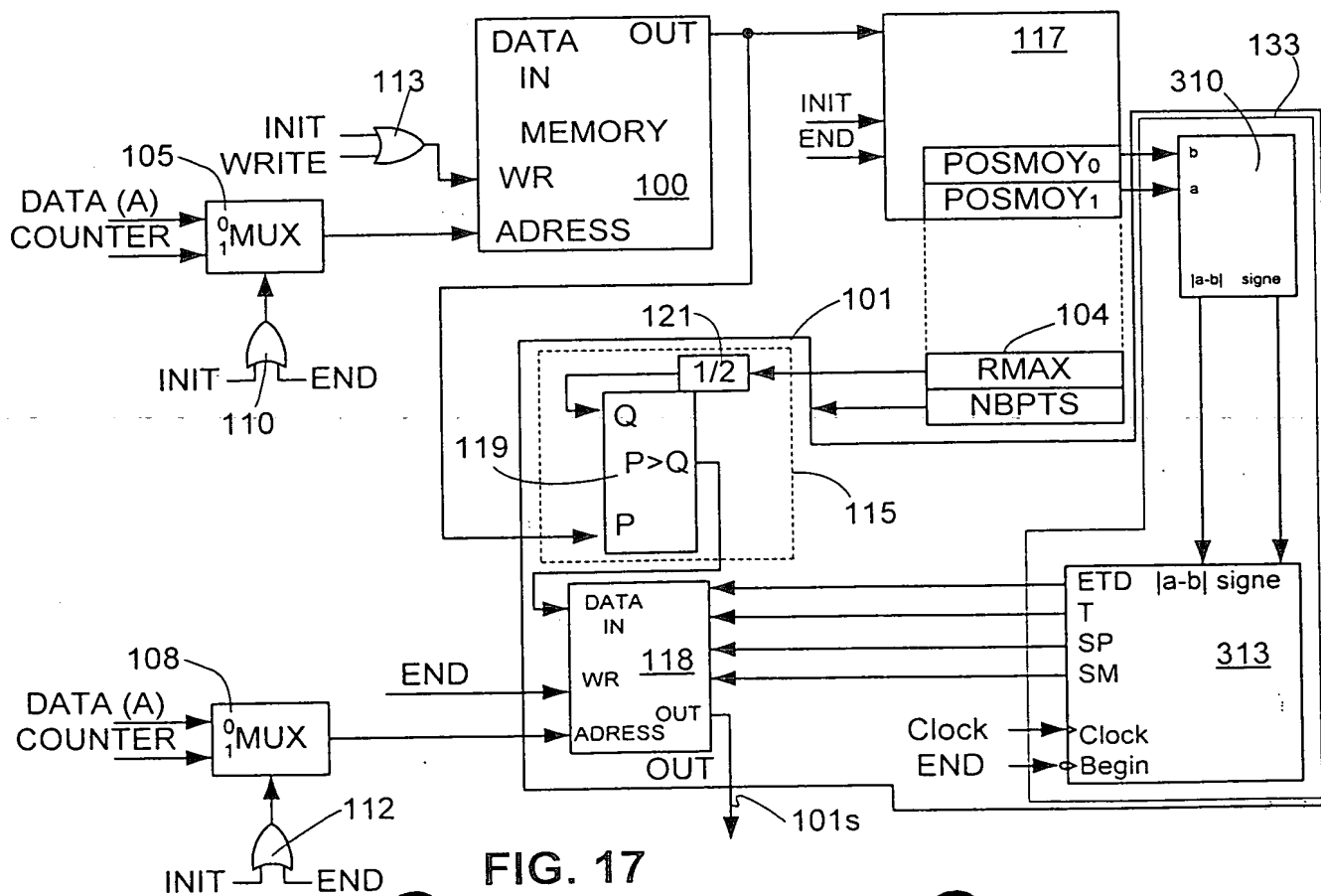
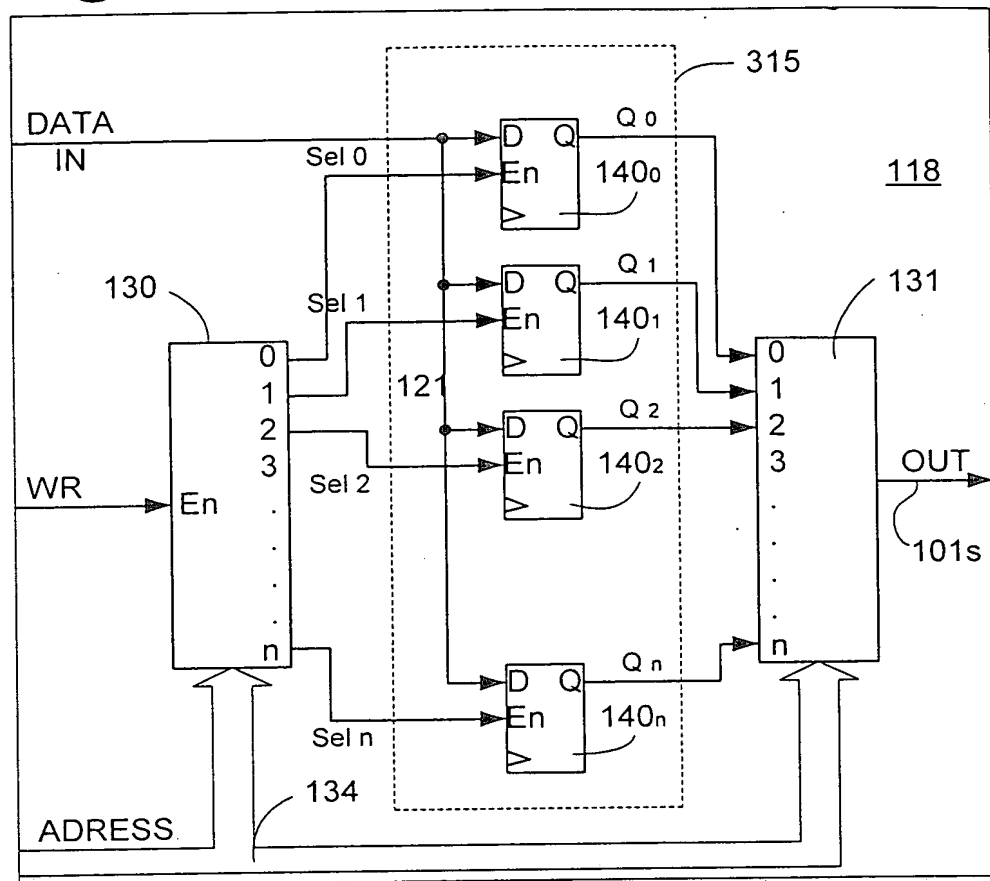


FIG. 17

FIG. 18

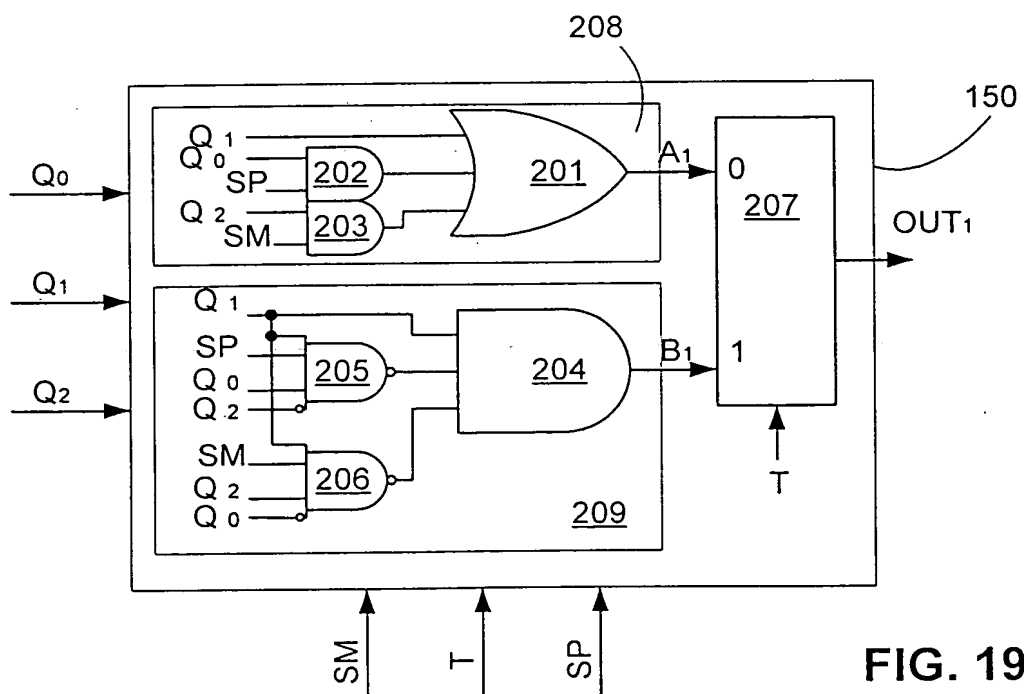
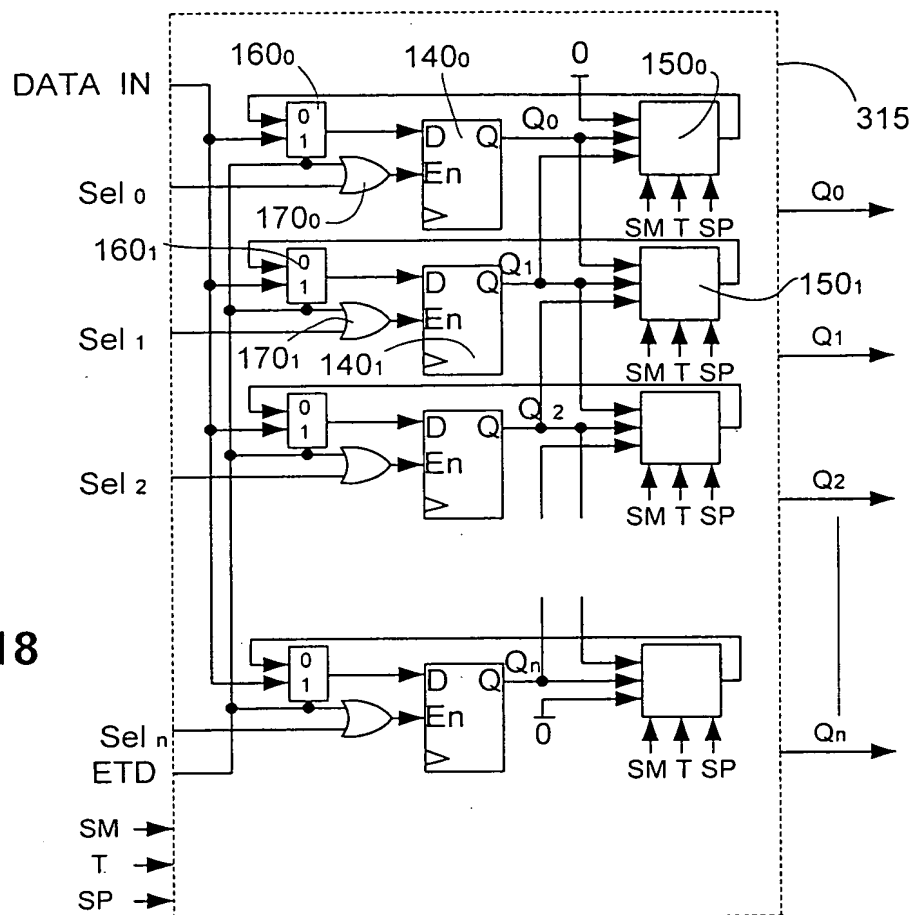


FIG. 19

FIG. 20

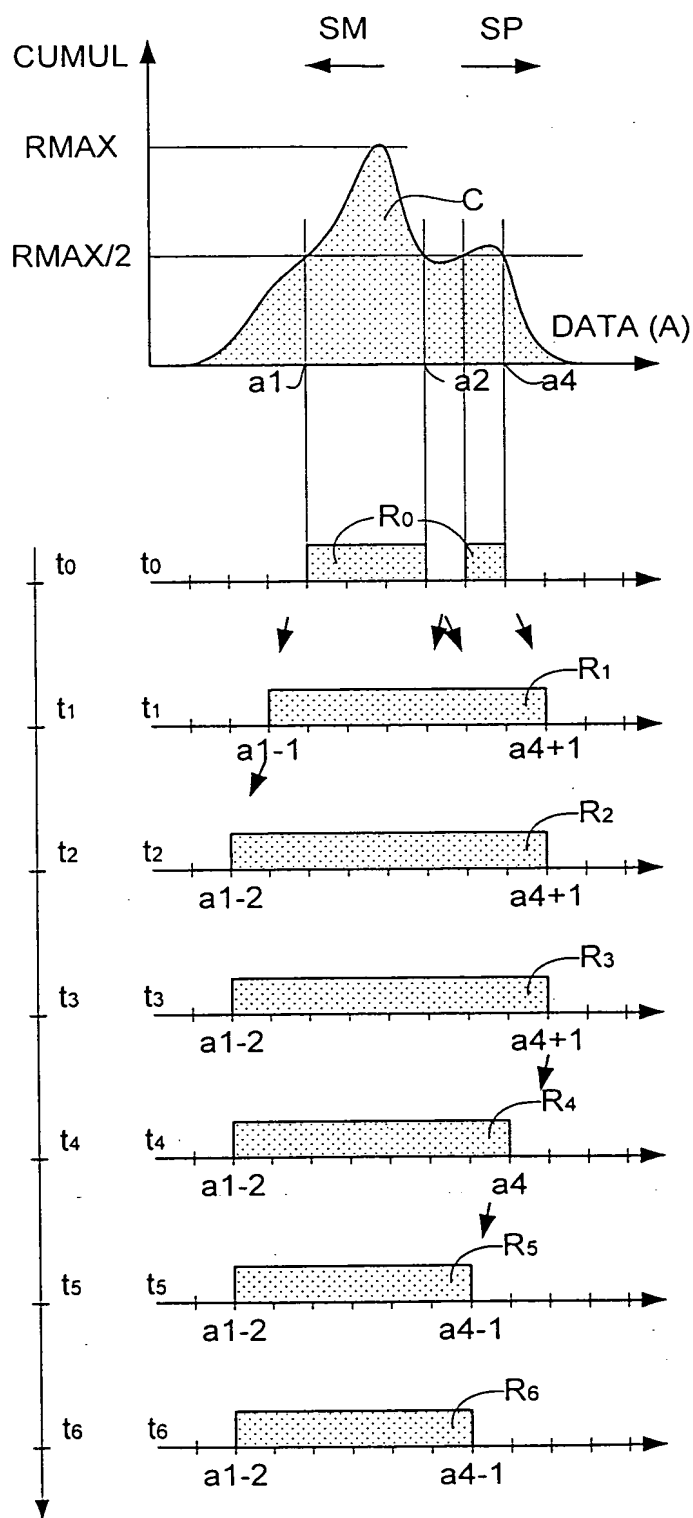
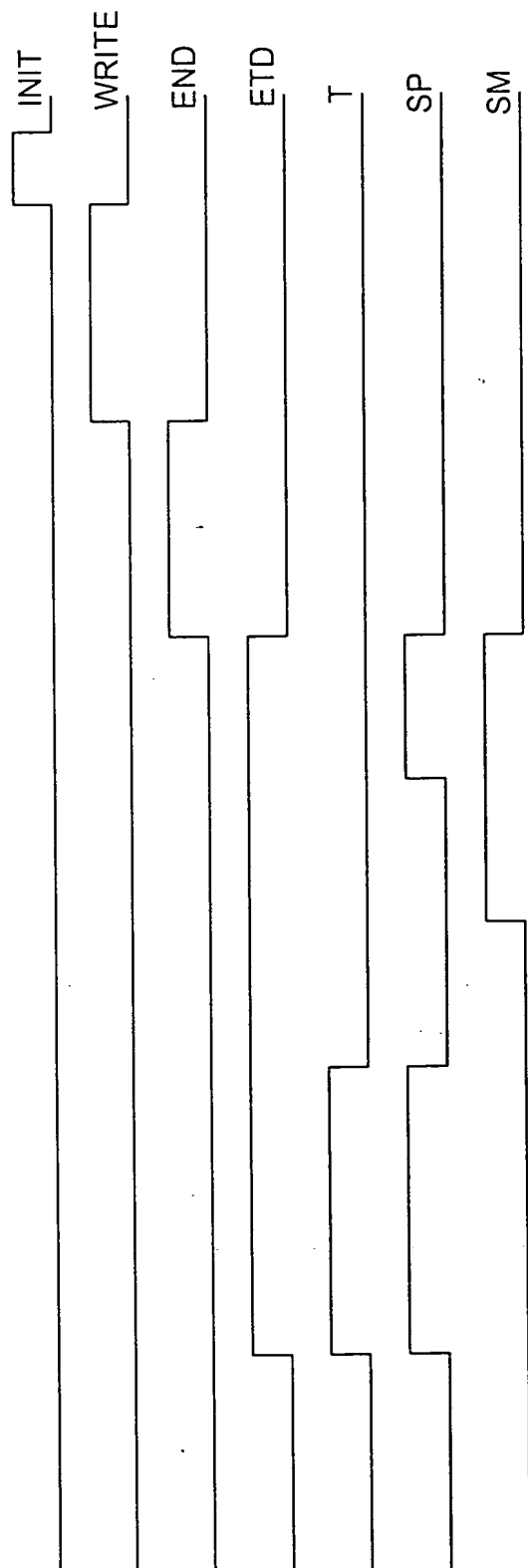
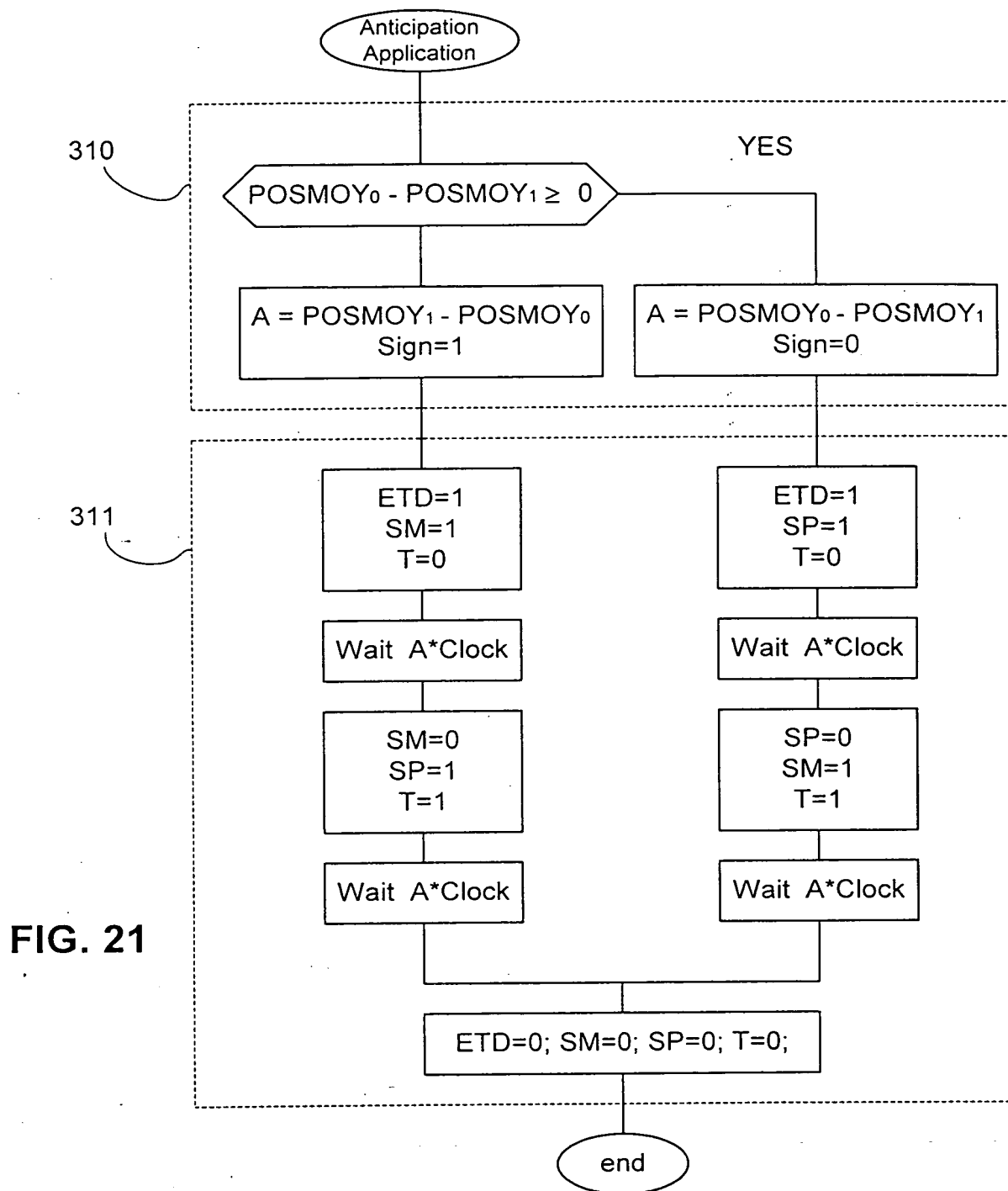


FIG. 20



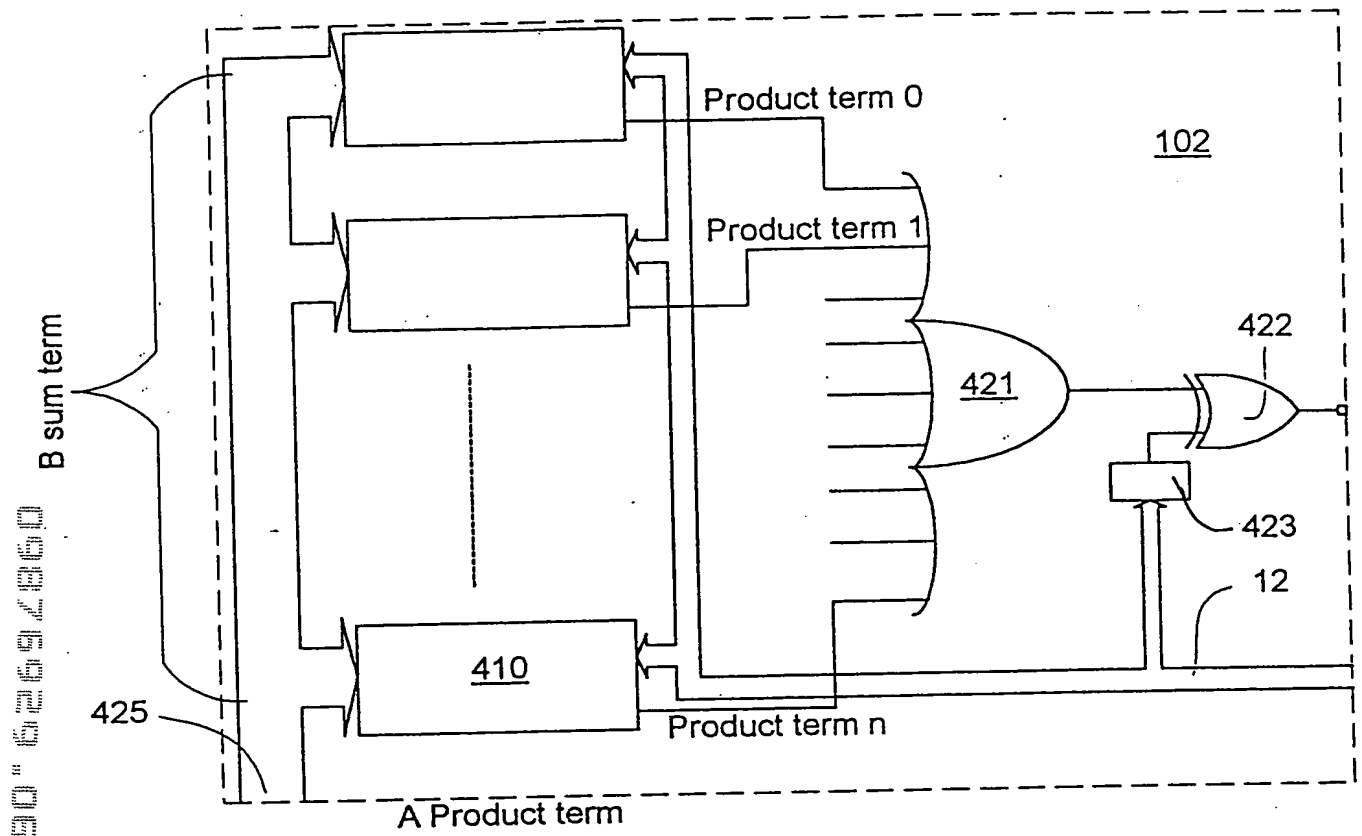


FIG 22

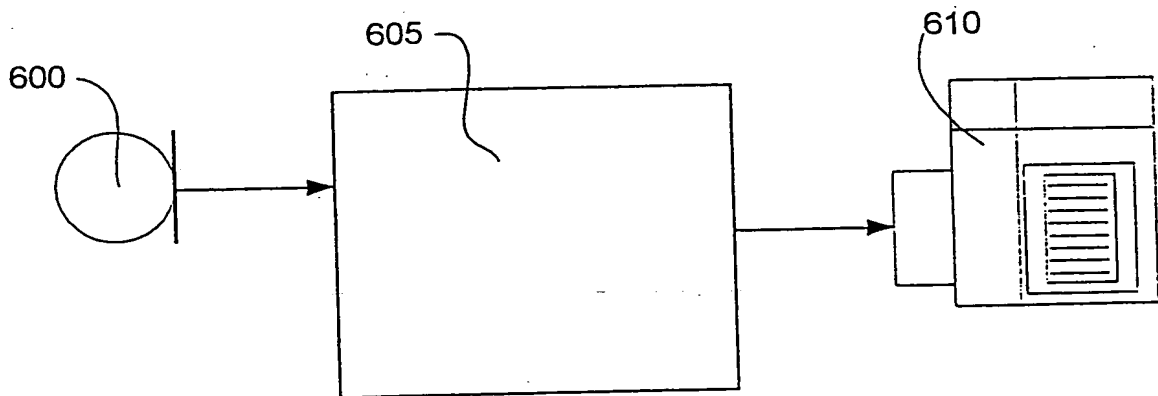


FIG. 39

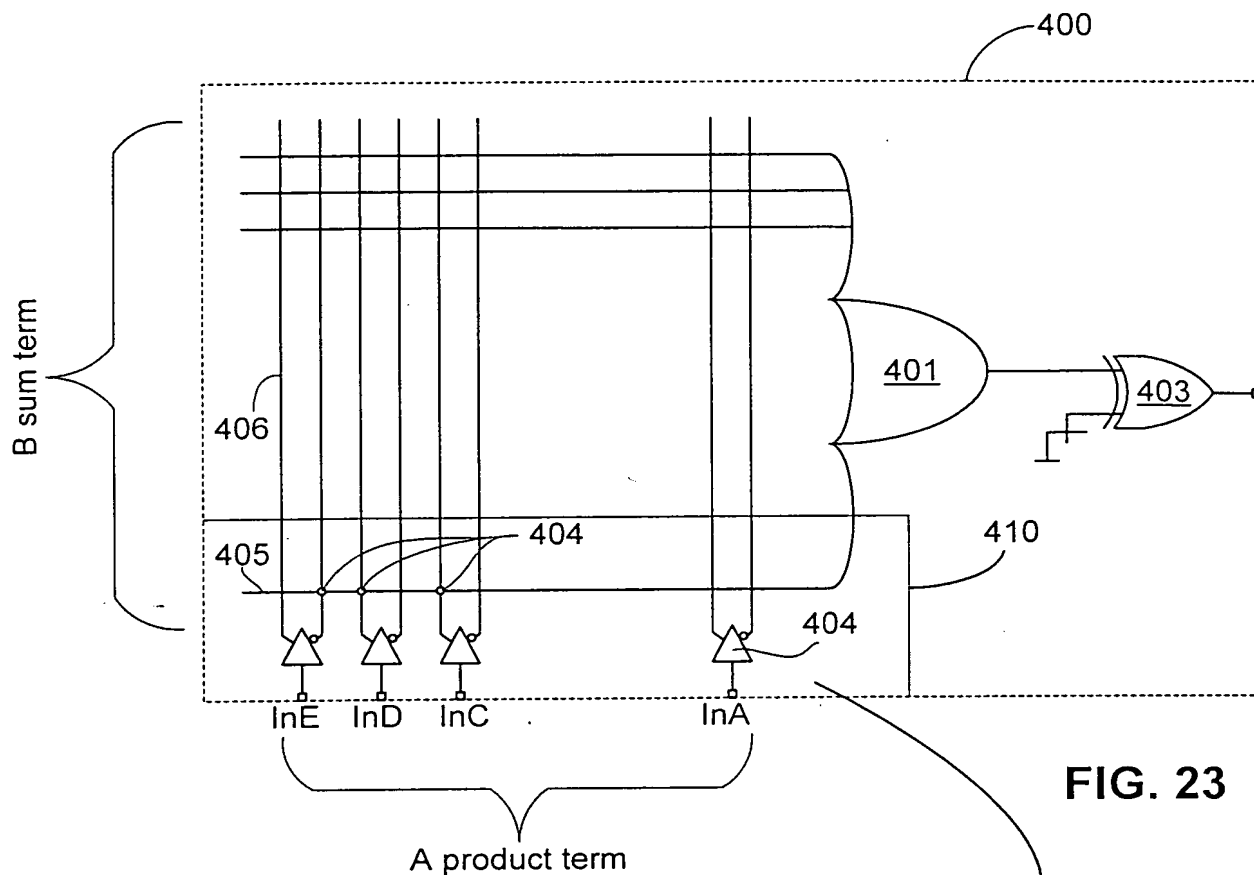


FIG. 23

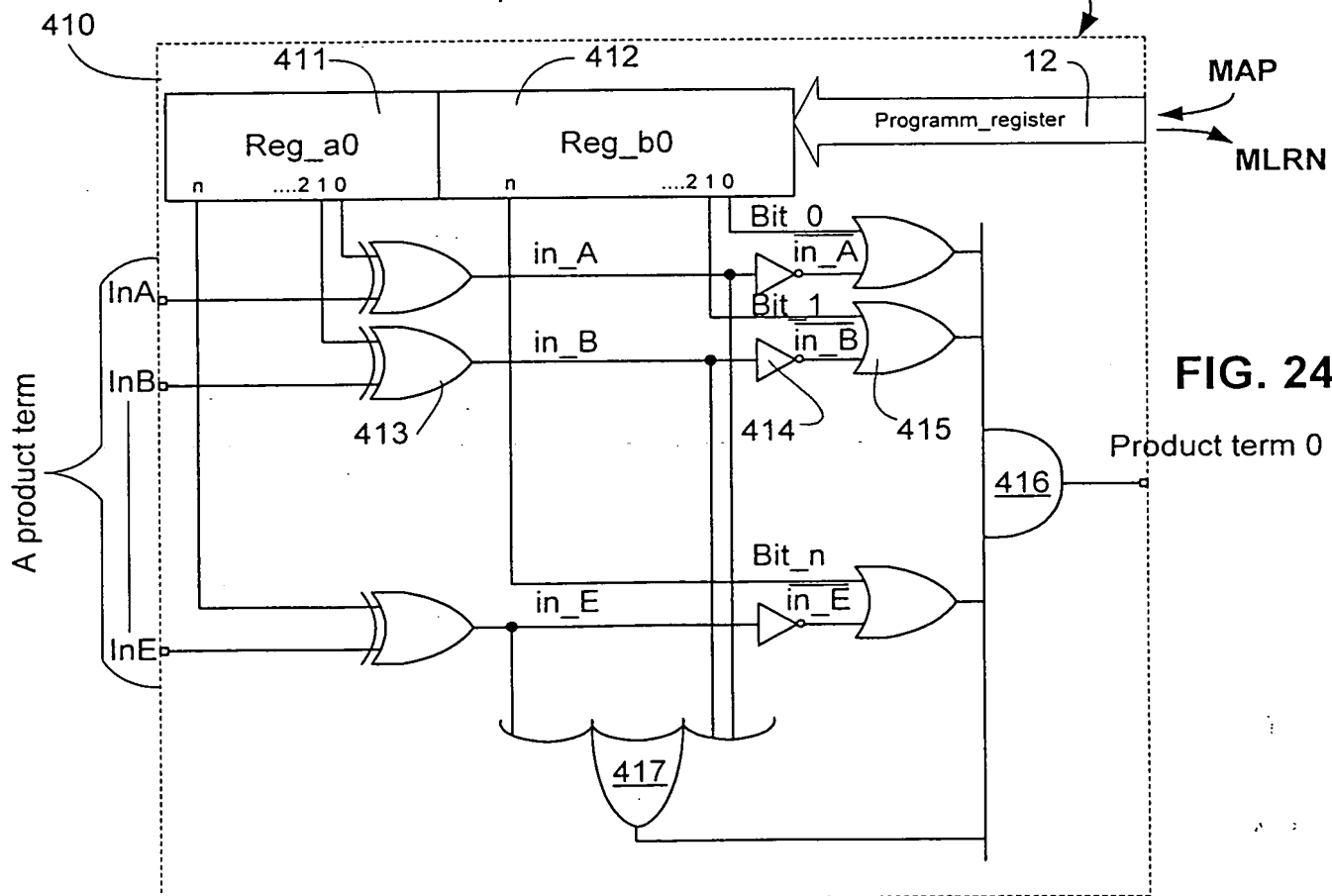


FIG. 24

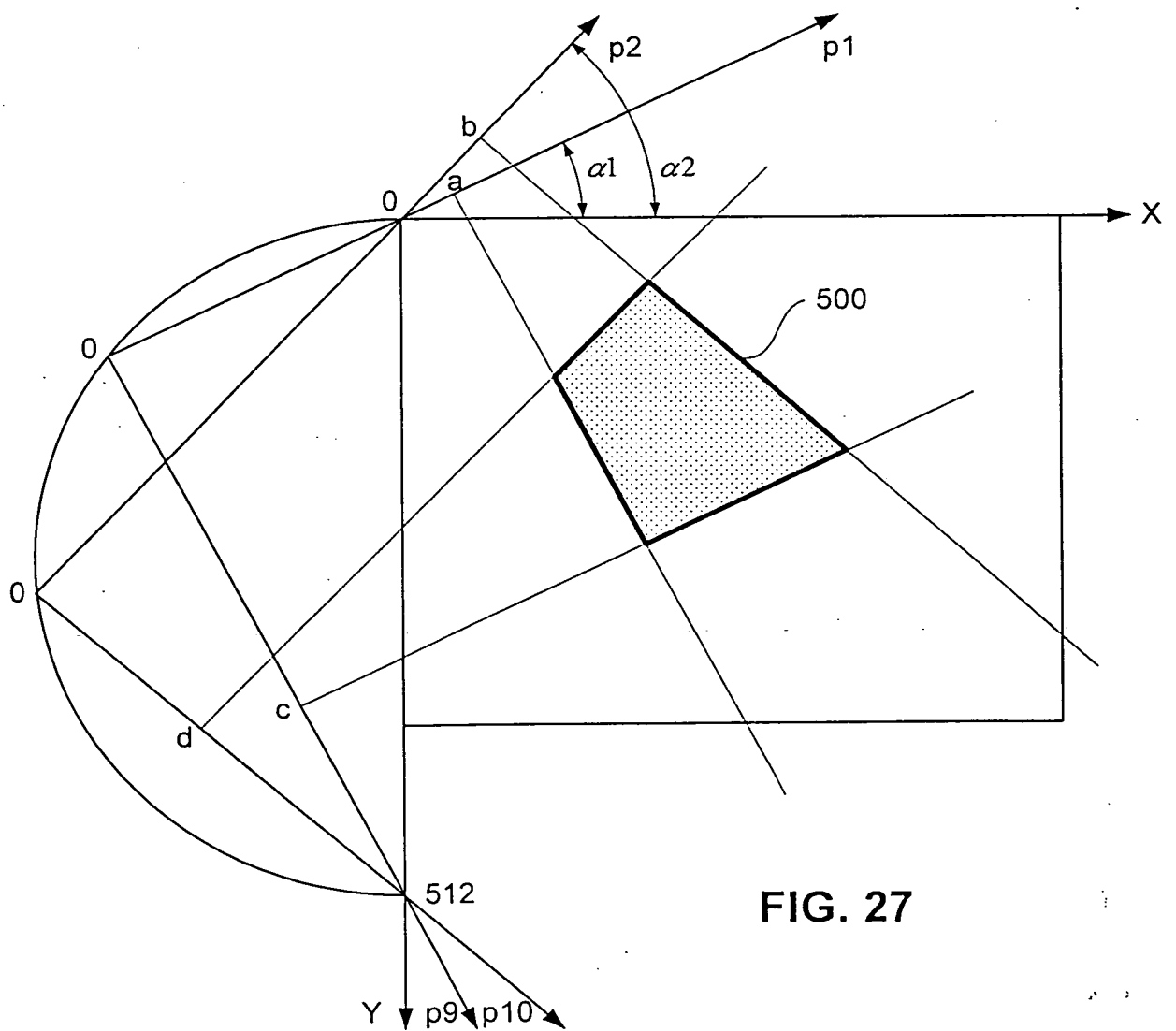
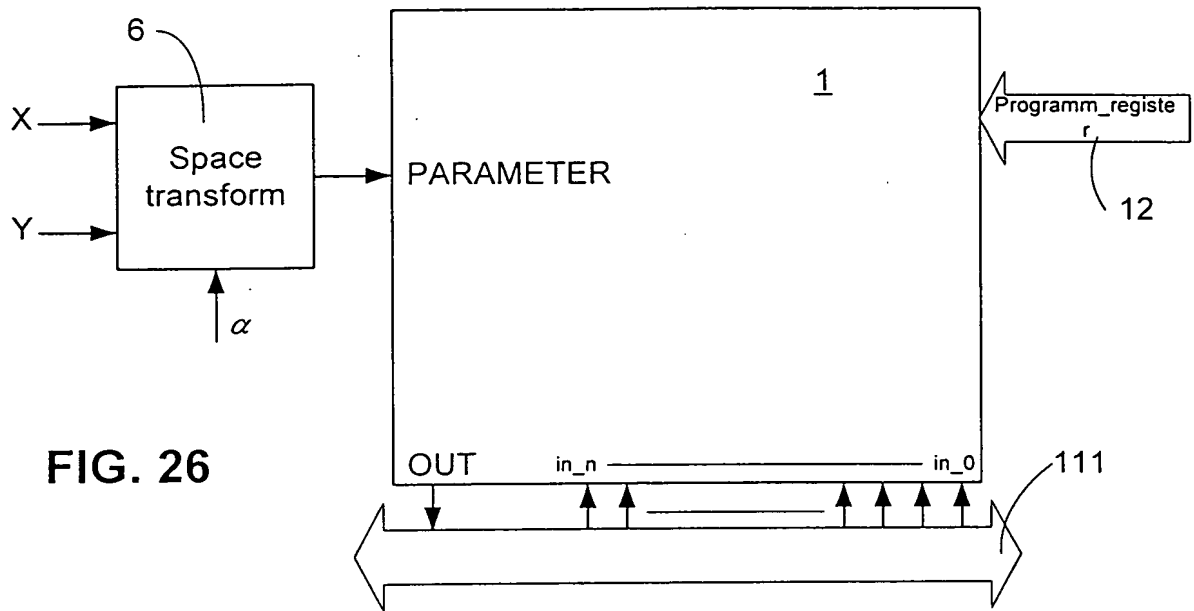


Fig. 28

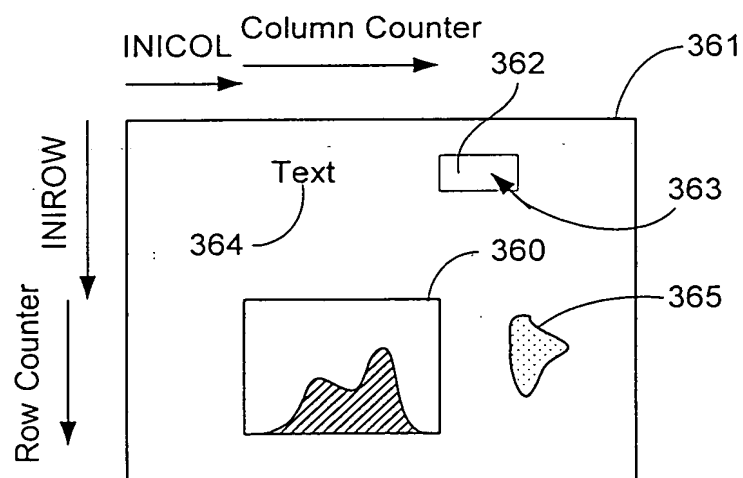


Fig. 29

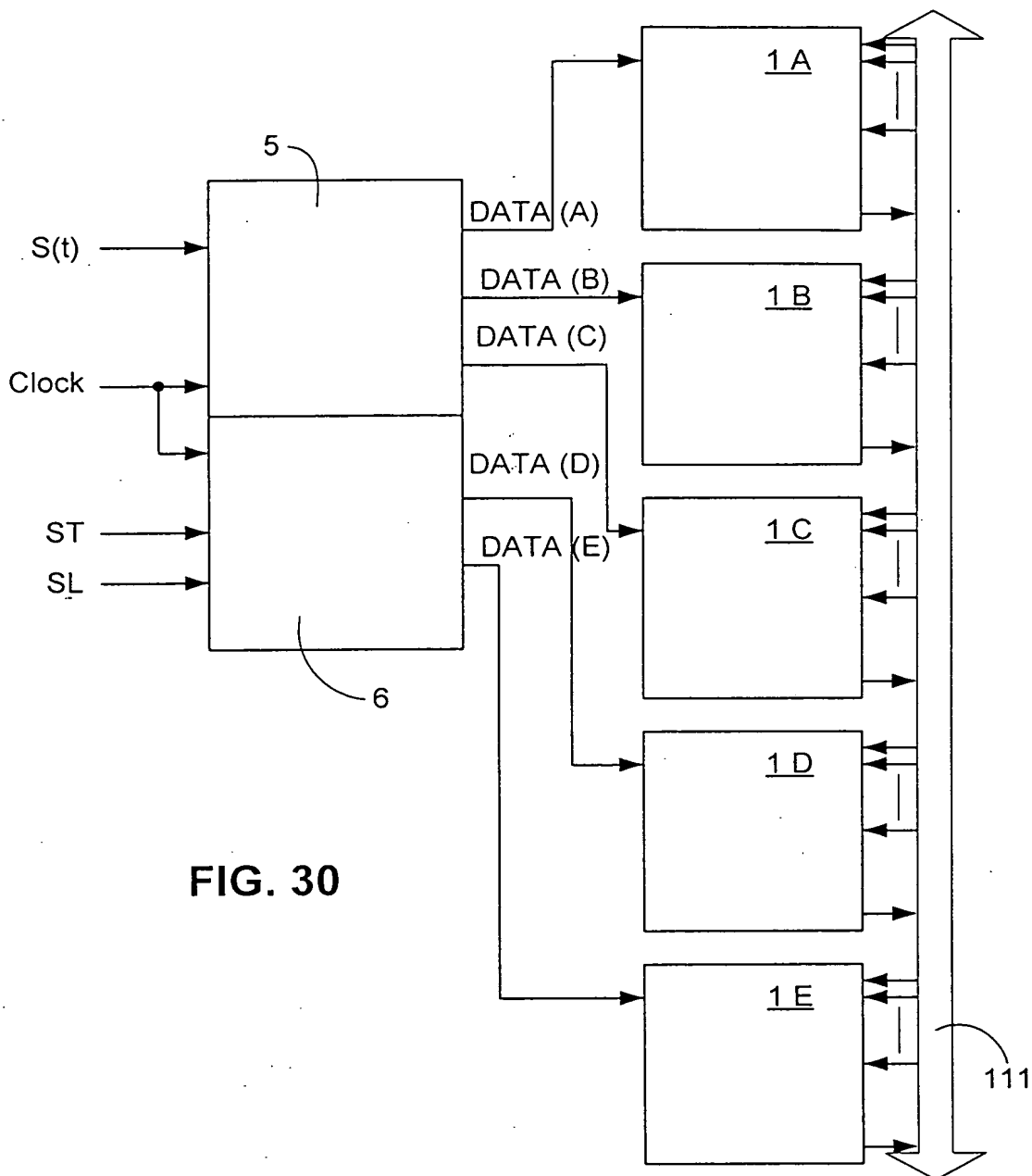


FIG. 30

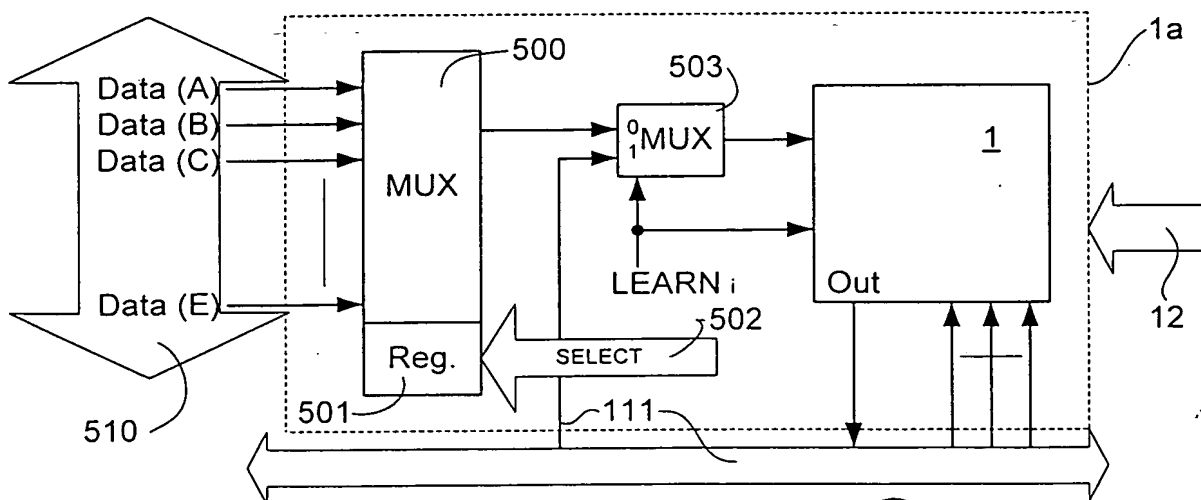


FIG. 31

FIG. 31a

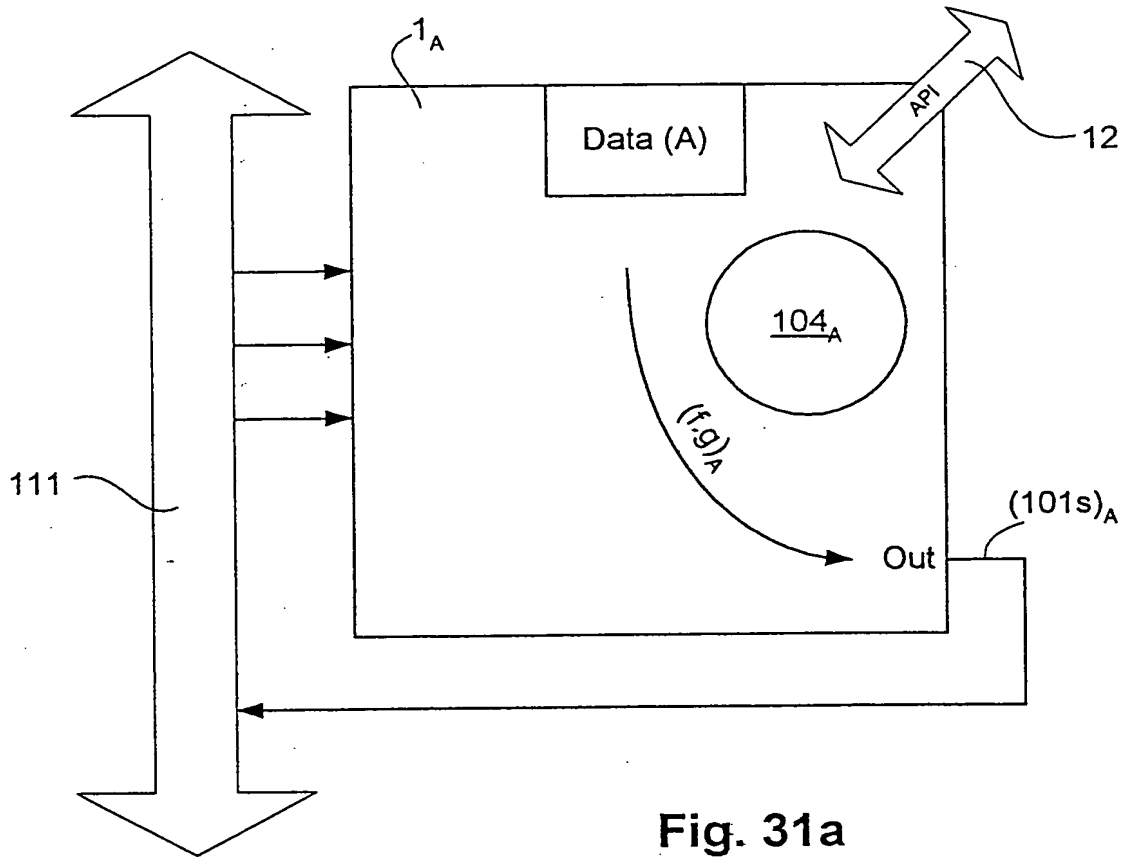


Fig. 31a

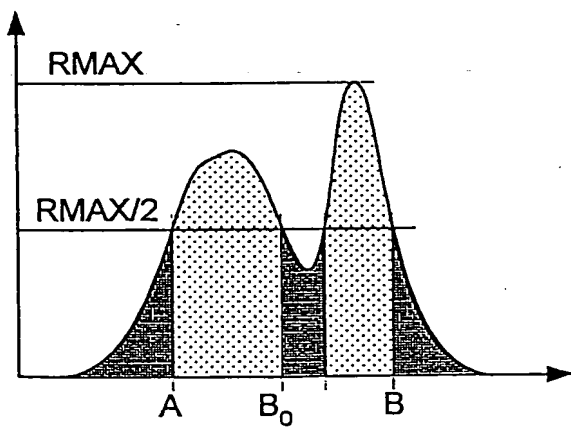


Fig 13a

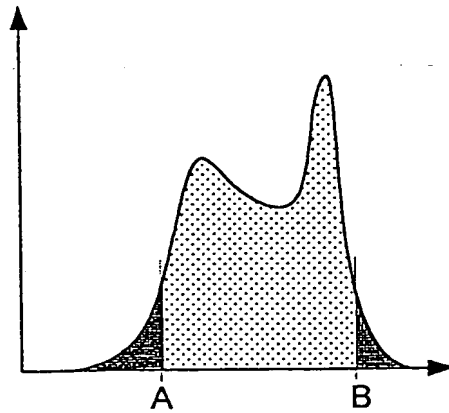


Fig 13b

FIG. 32

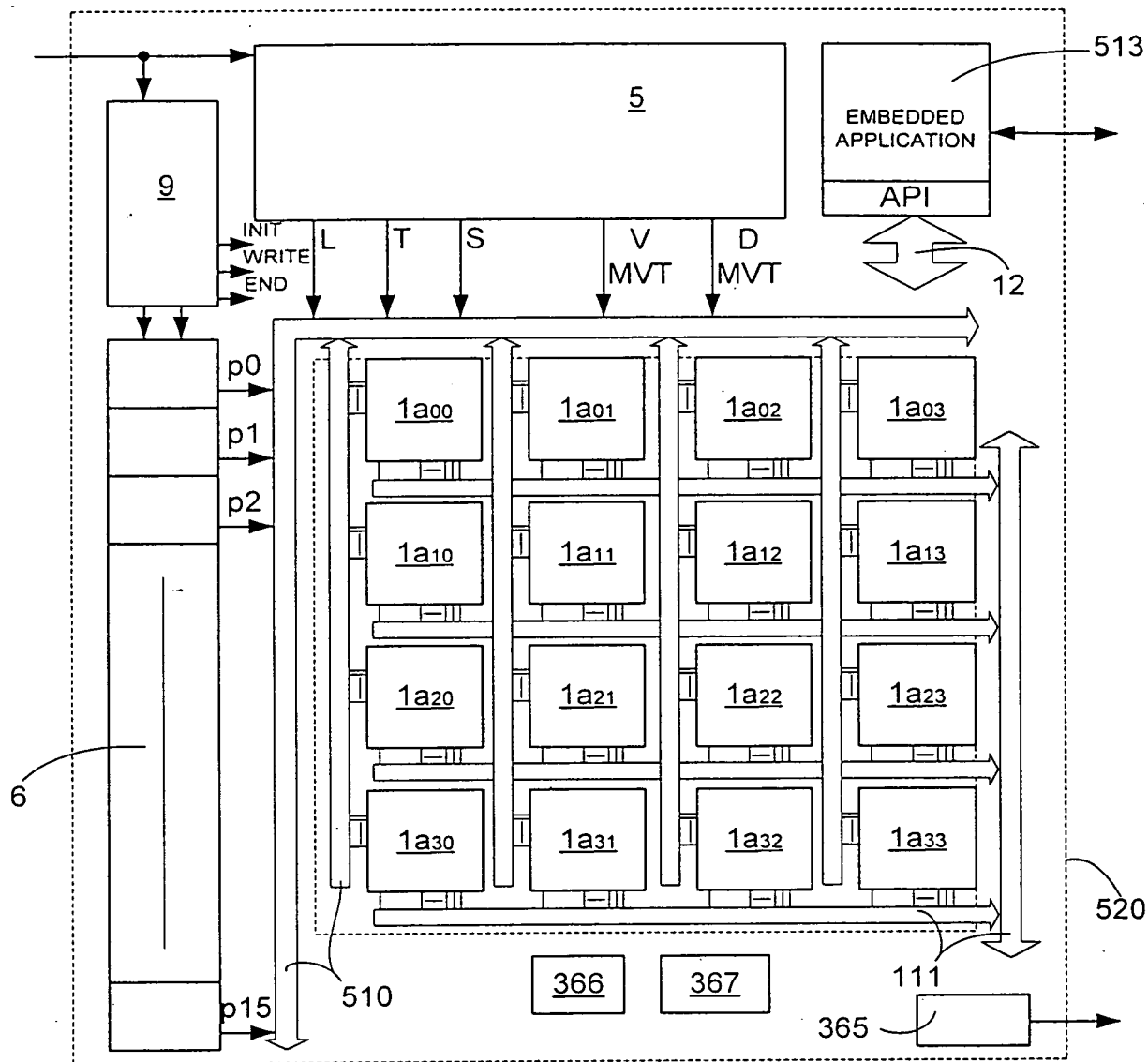


FIG. 32

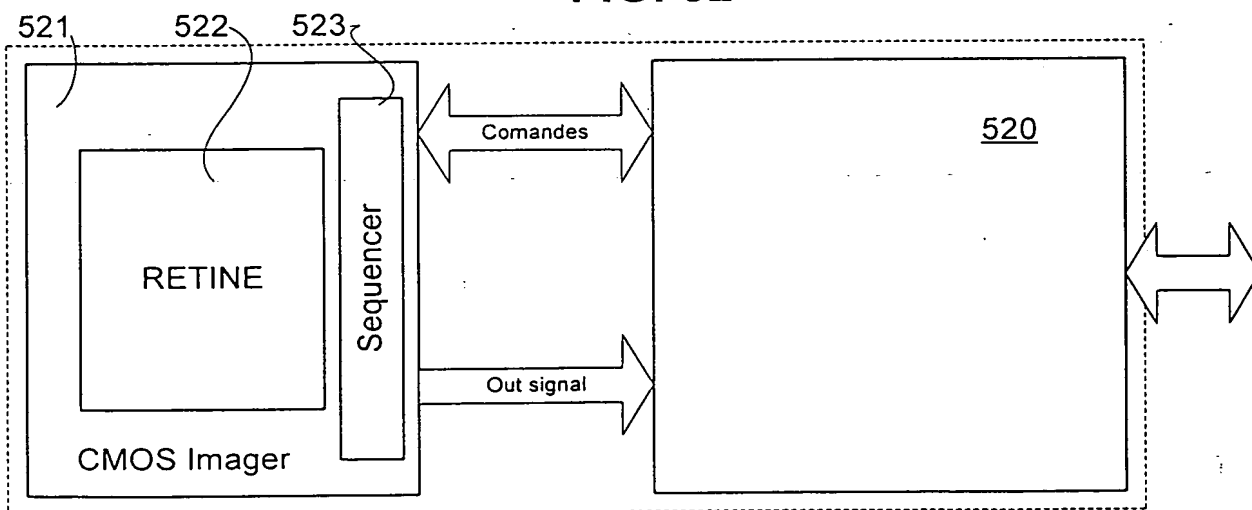


FIG. 33

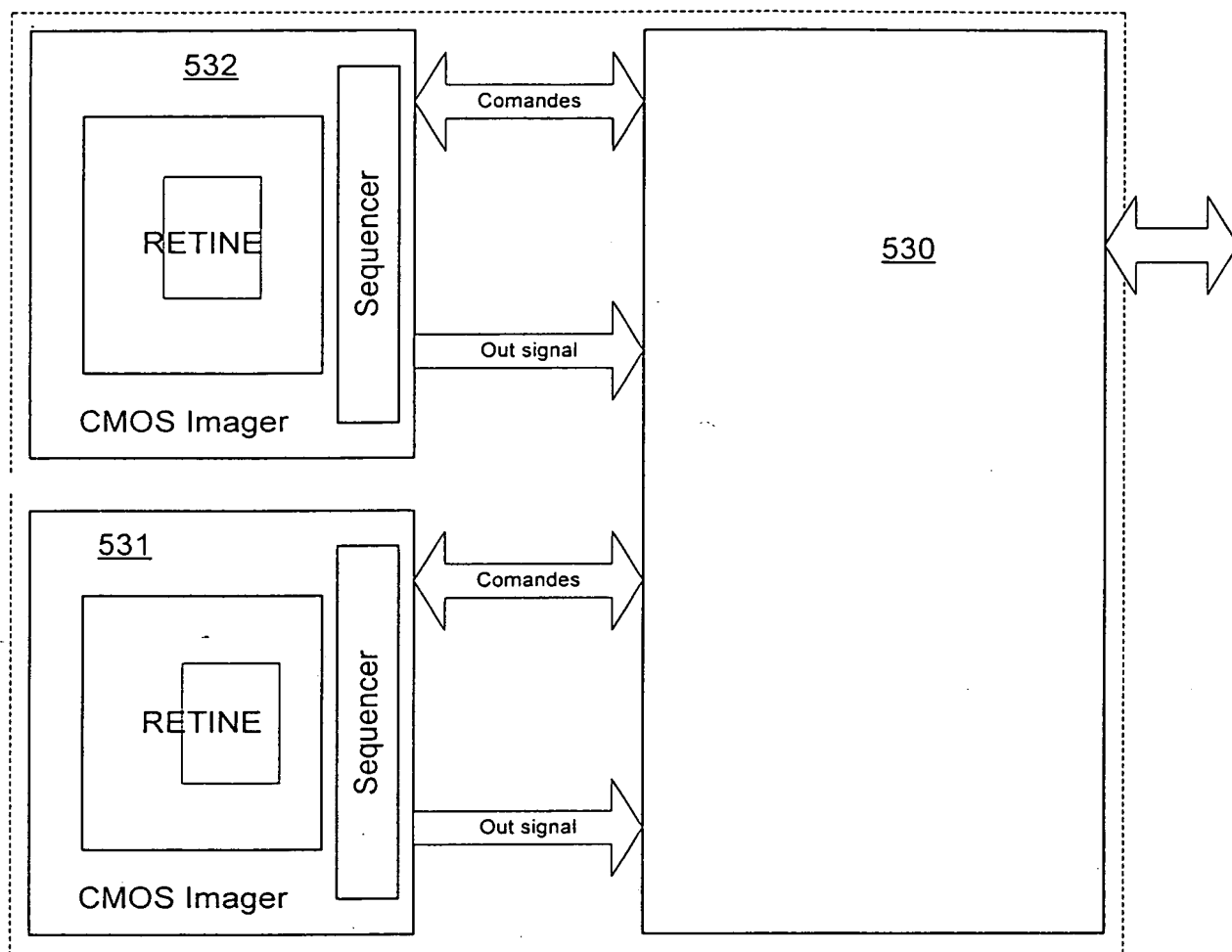


FIG. 35

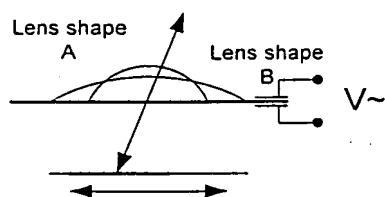
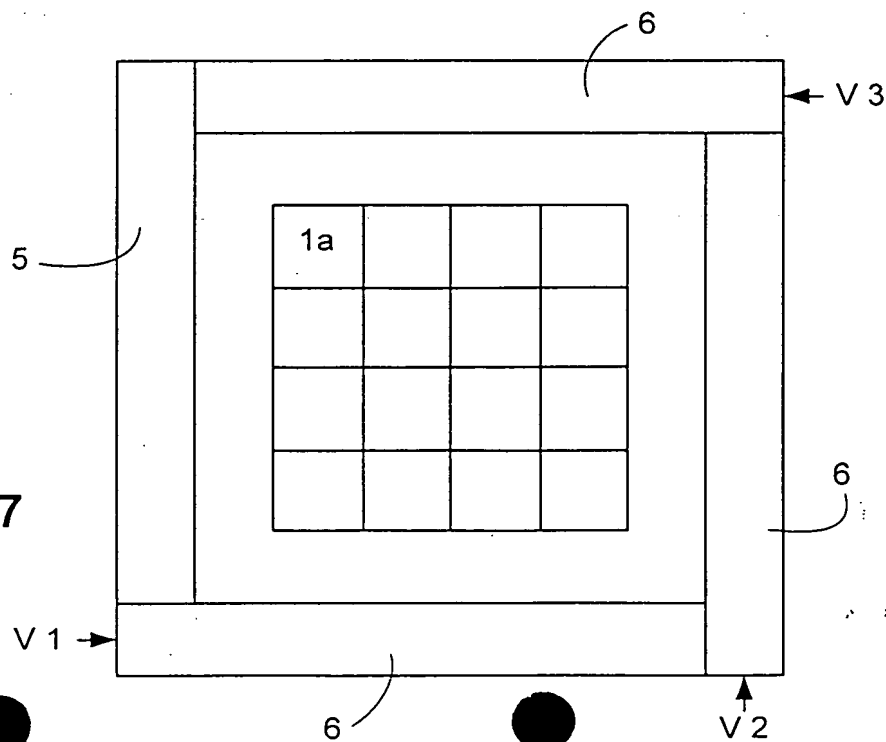


FIG. 36

FIG. 37



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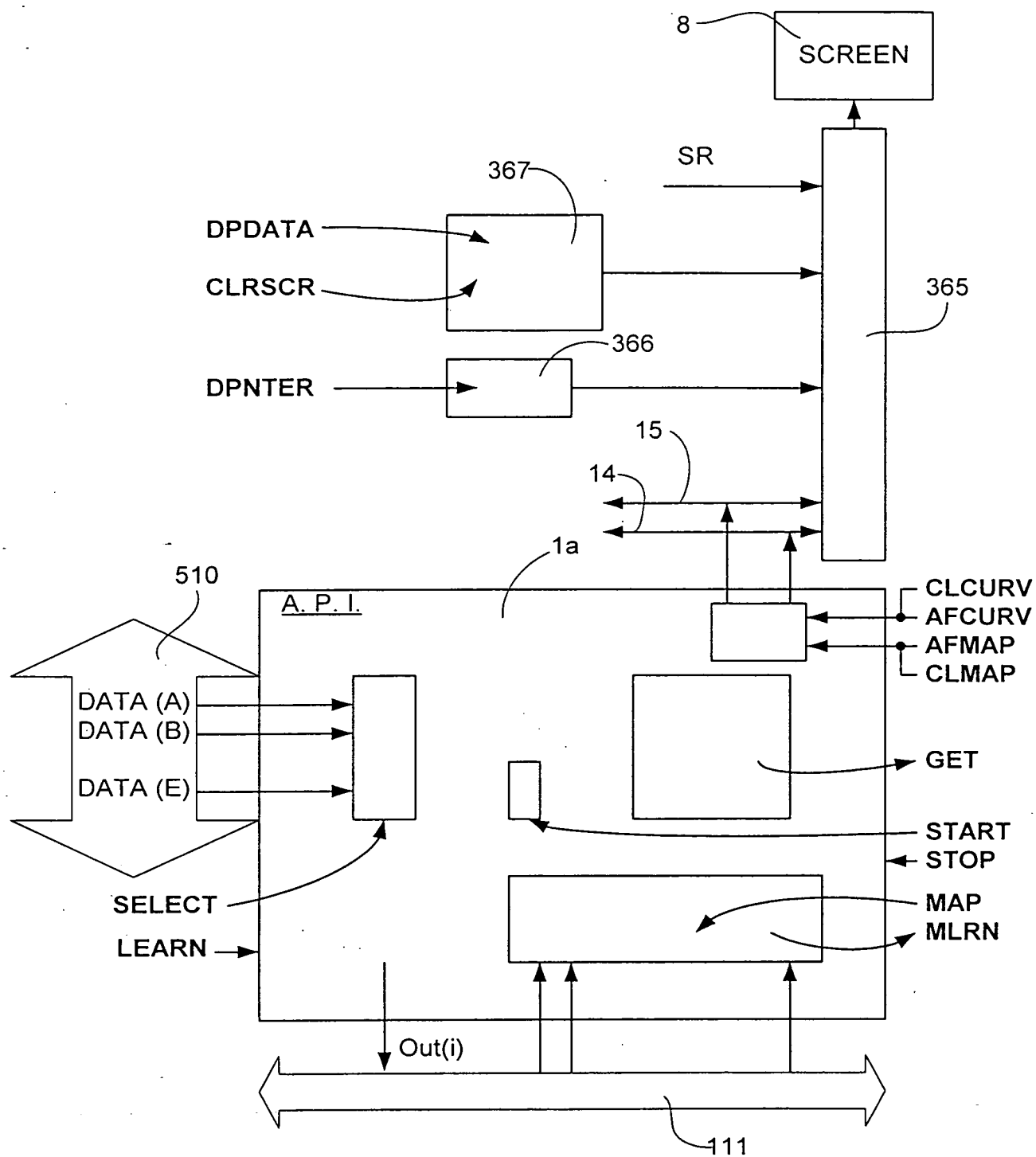


FIG. 38

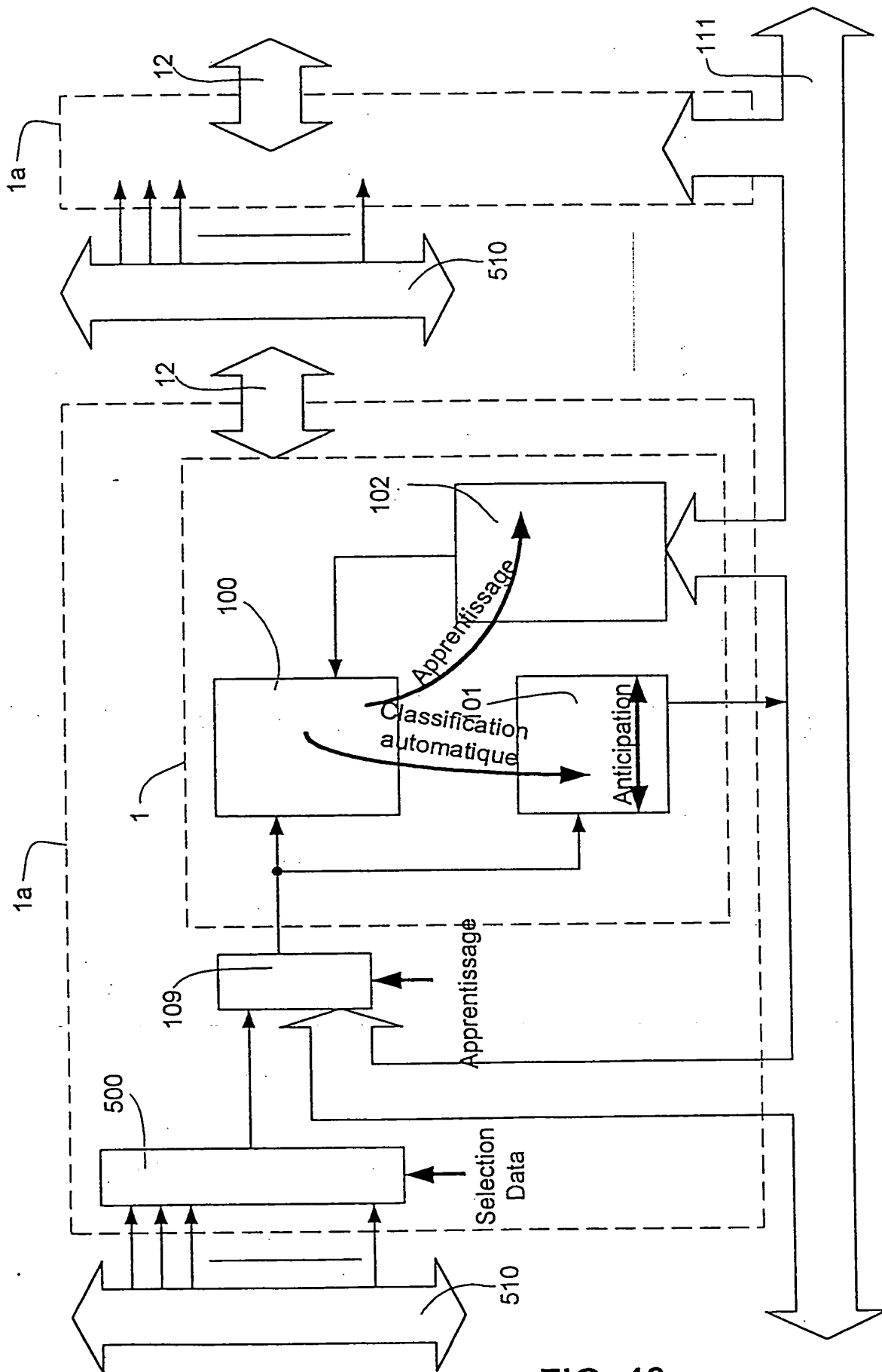


FIG. 40

FIG. 41

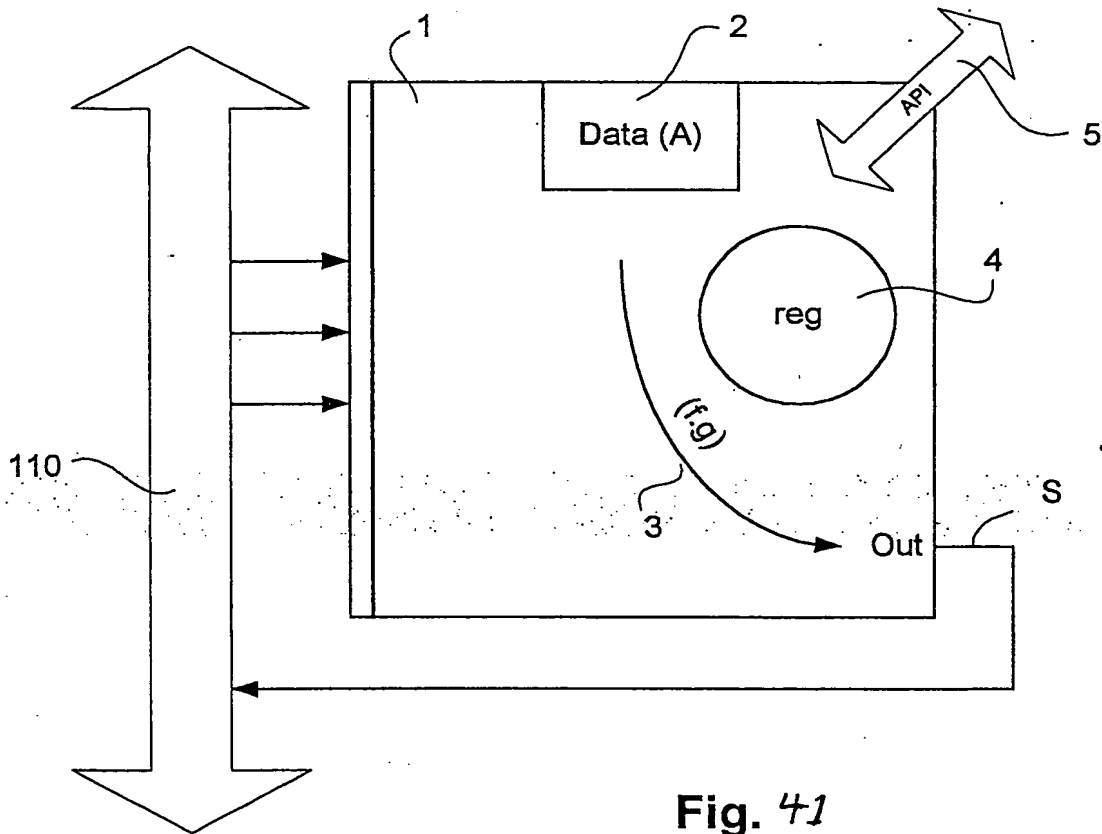


Fig. 41

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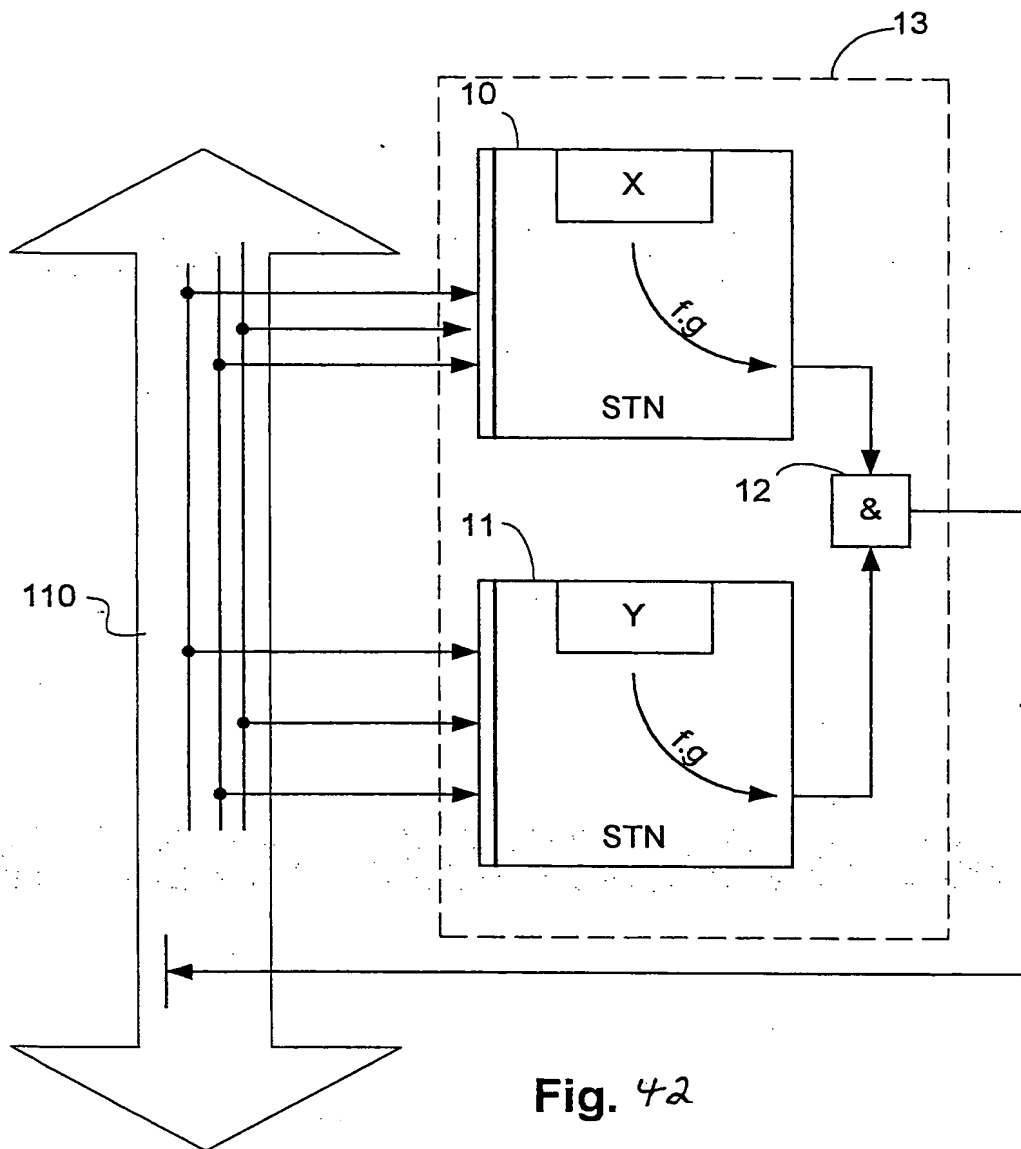


Fig. 42

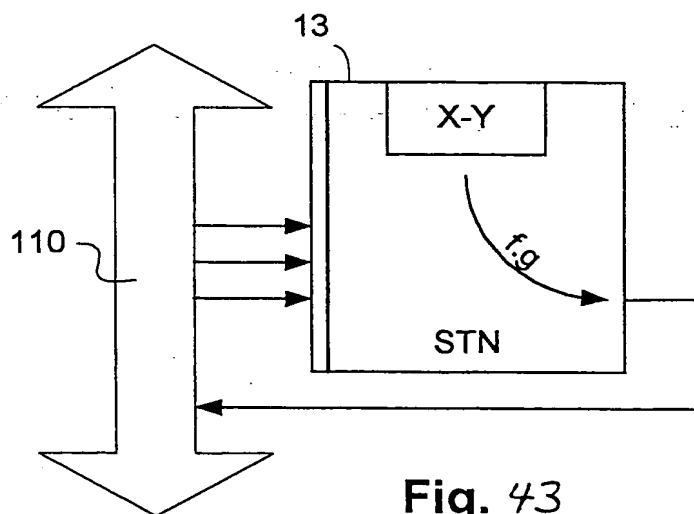


Fig. 43

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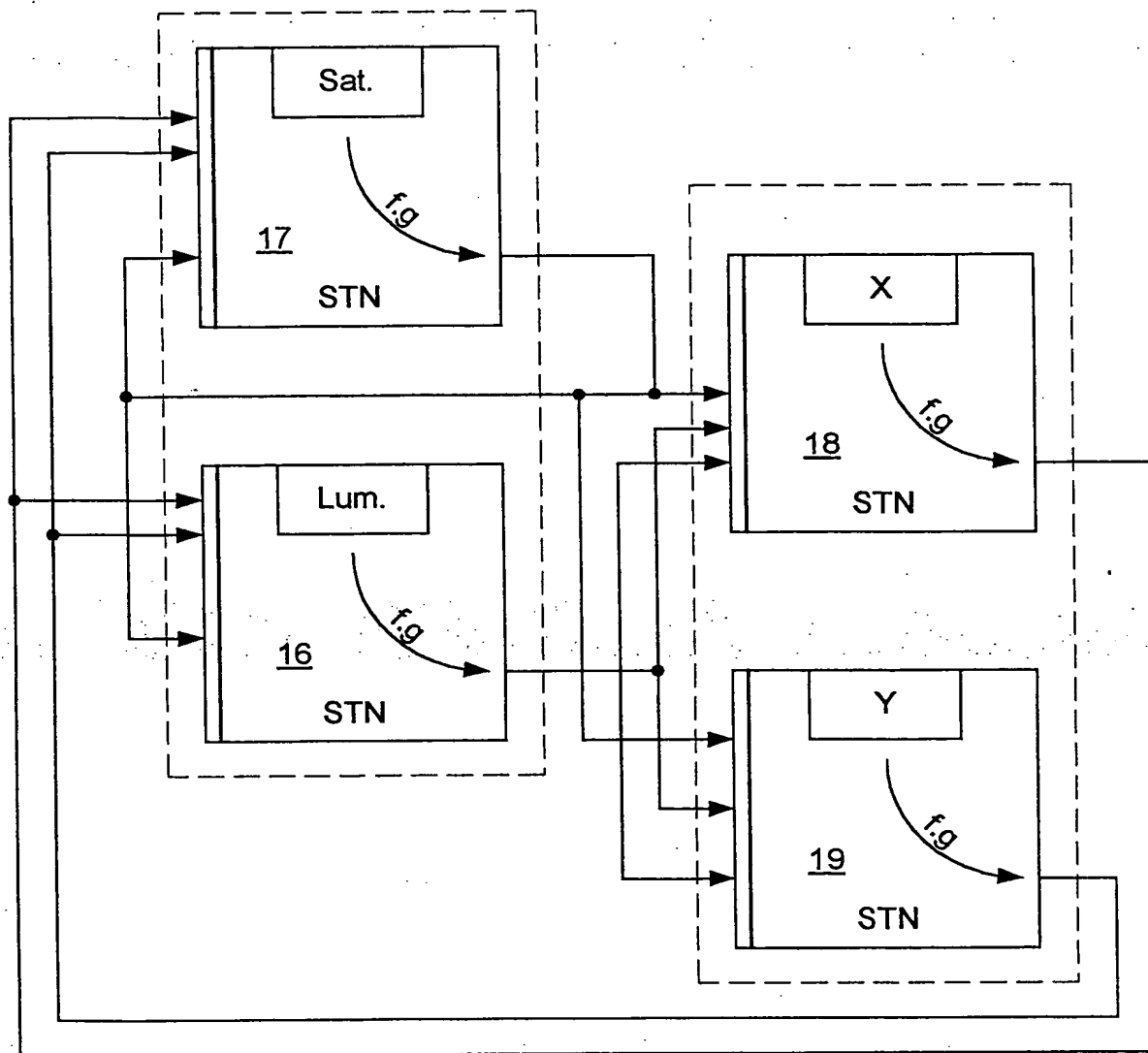


Fig. 44

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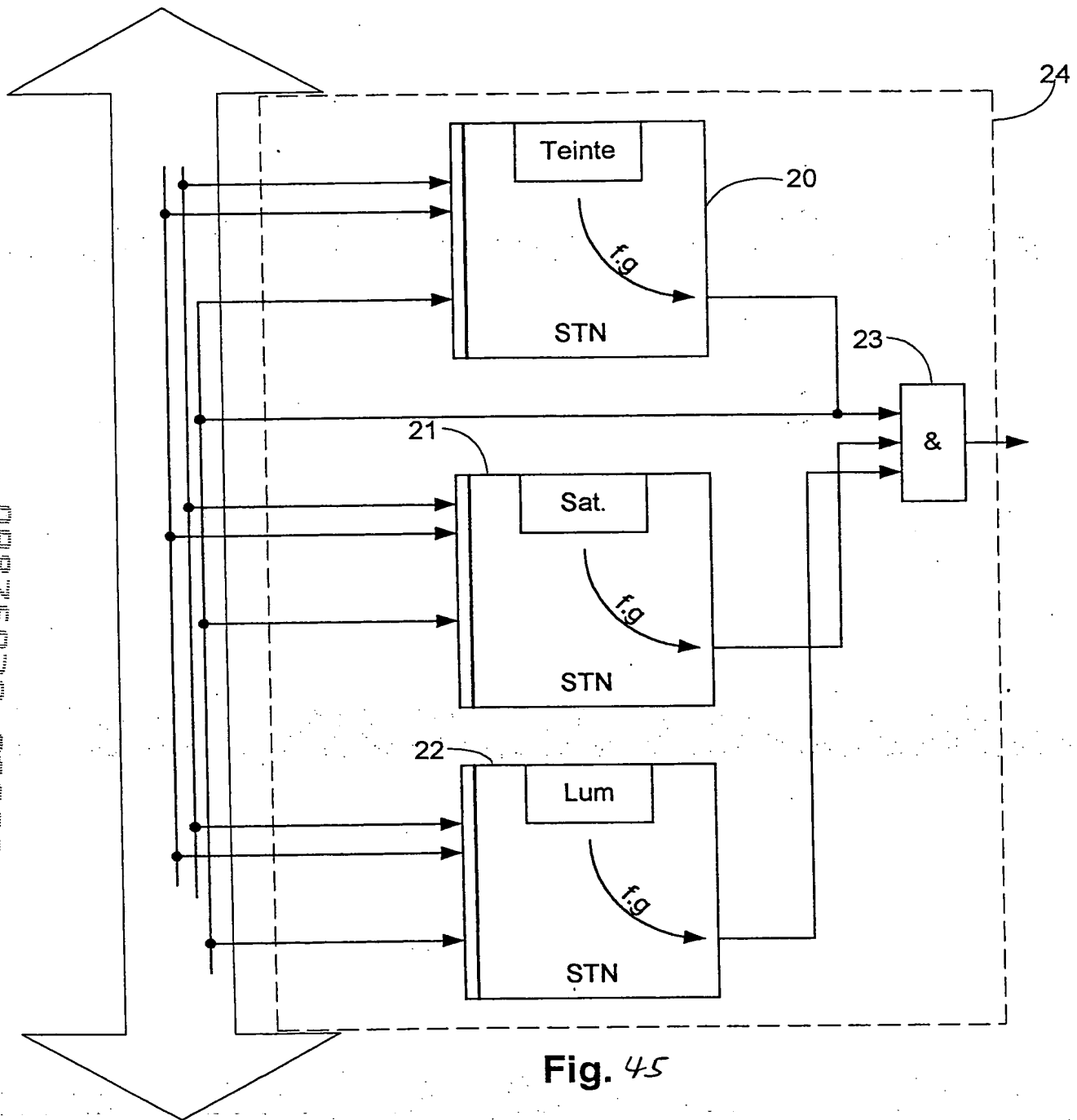


Fig. 45

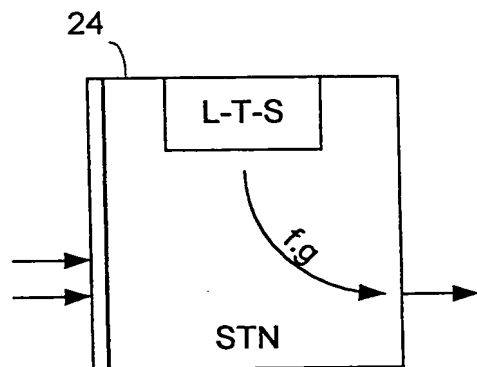


Fig. 46

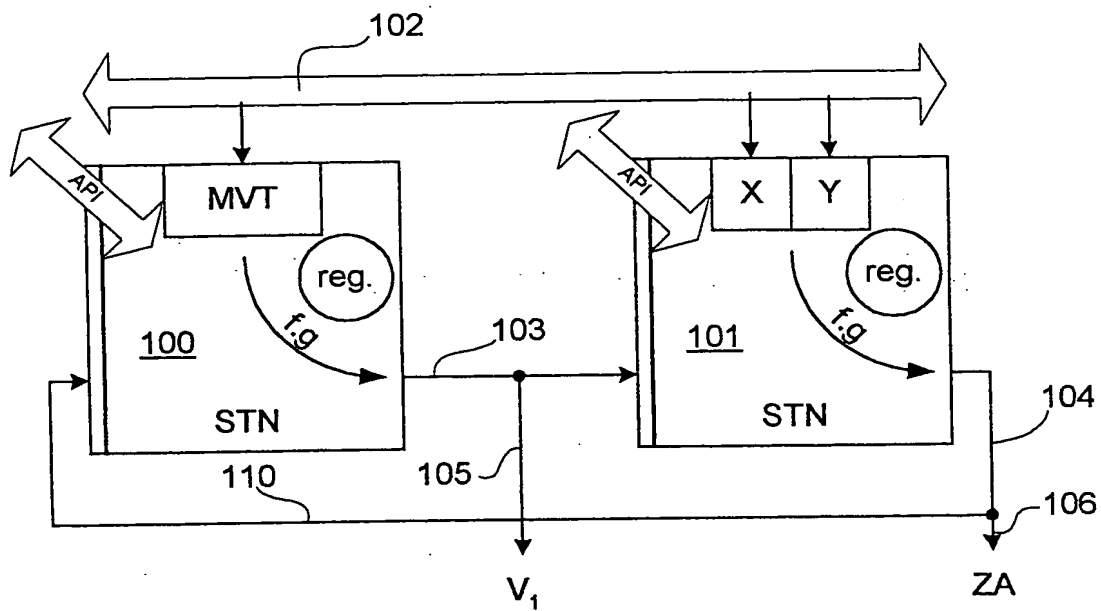


Fig. 47

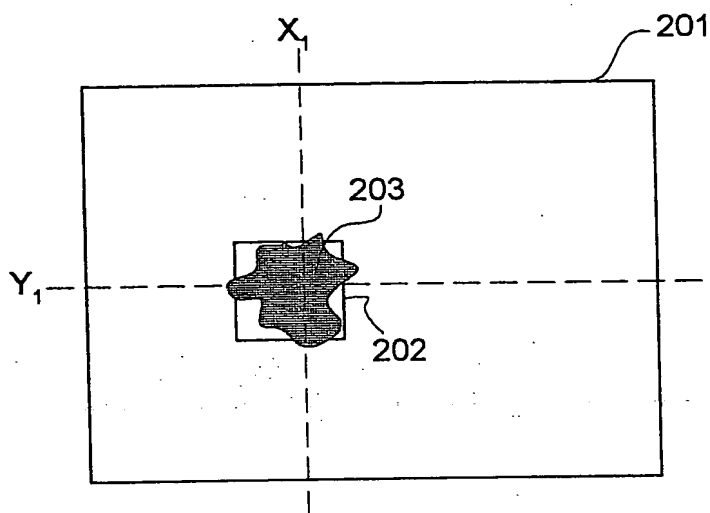


Fig. 48

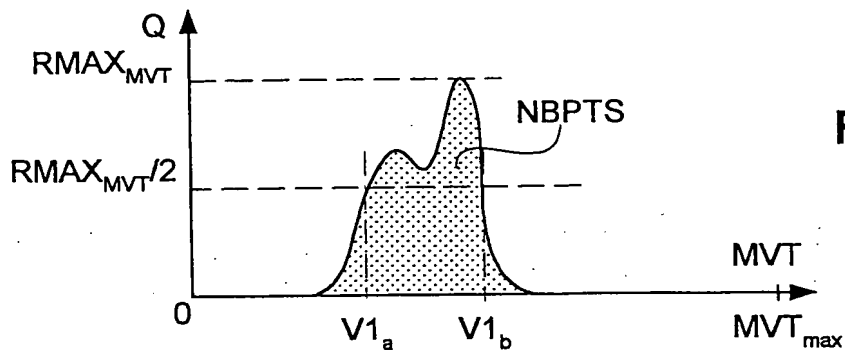


Fig. 49a

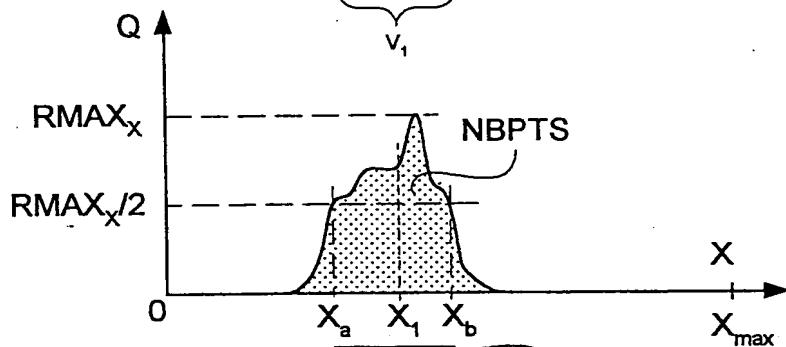


Fig. 49b

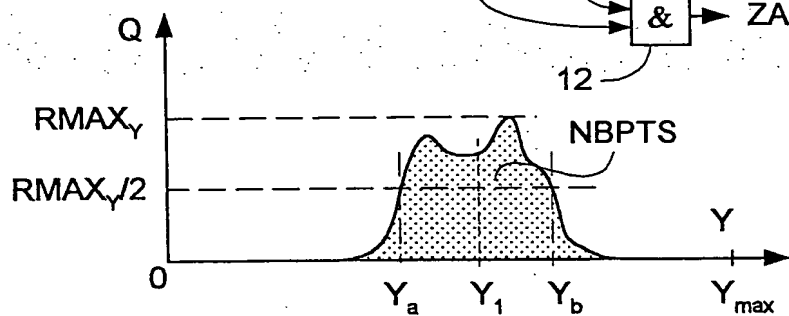


Fig. 49c

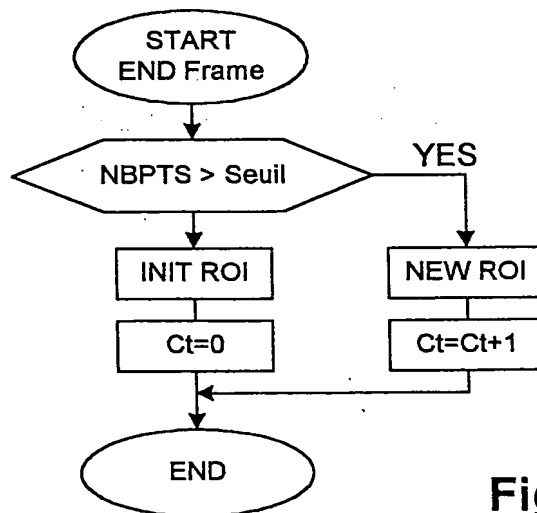


Fig. 50

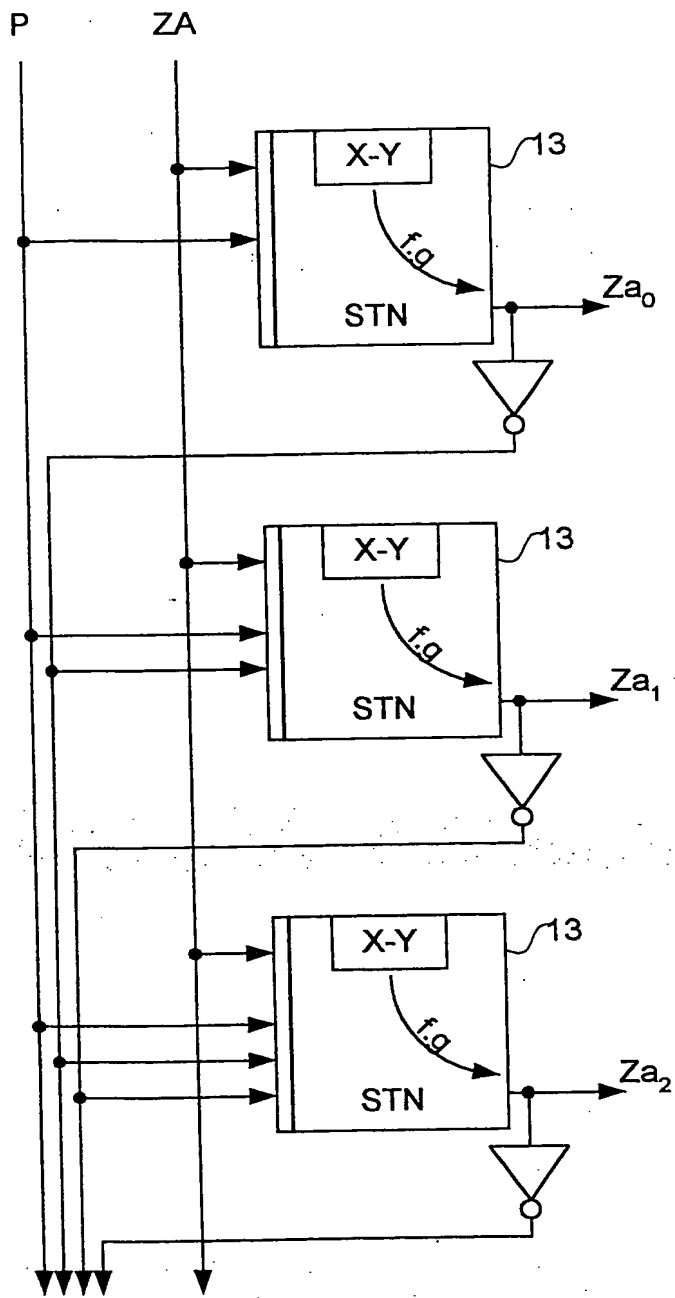


Fig. 51

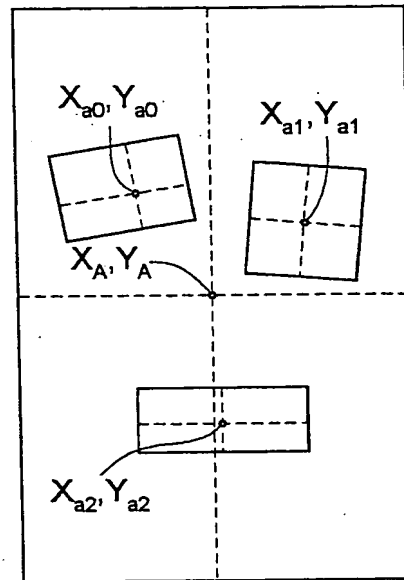


Fig. 54

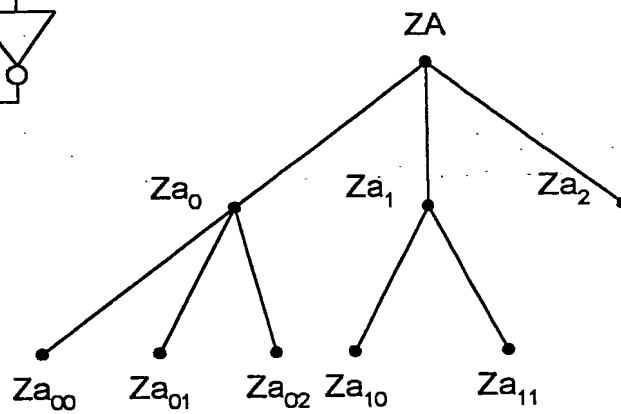


Fig. 52

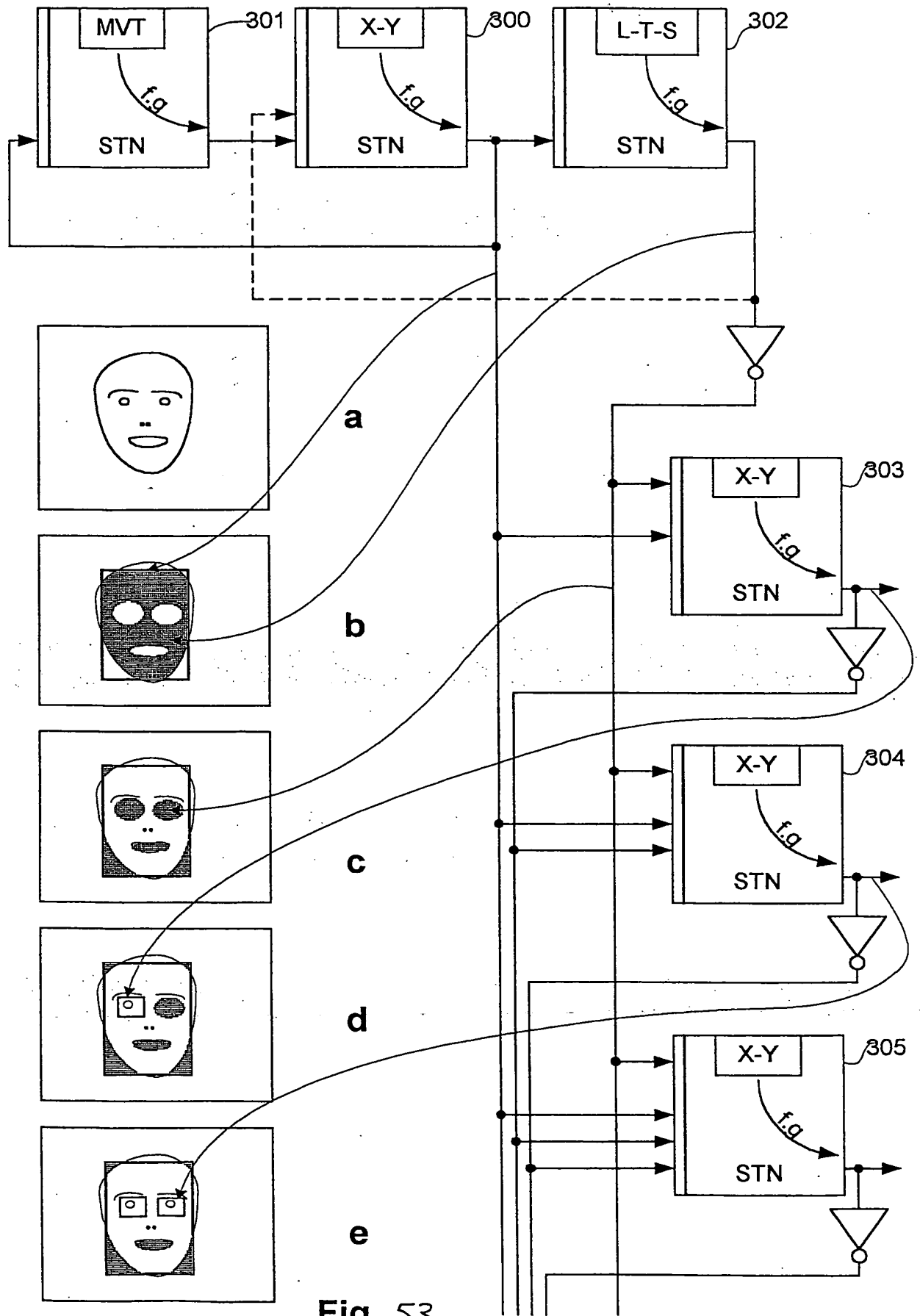


Fig. 53